COURSE GUIDE

IFT236
ANALOG AND DIGITAL ELECTRONICS

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Introduction

Analogue and digital electronics are the central core of computing and computer systems. They provide the basis on which useful electronic systems are designed and built. It is against this backdrop that this course i.e. Analogue and Digital Electronics – a 3 credit unit course introduces the student to aspects of analogue and digital electronics with a view to enabling the student develop a basic competence in the subject area. Consequently, the student is introduced to the principle of operation and application of analogue and digital electronic components. The components that will come under focus include but not limited to amplifiers, filters, oscillators, analog-to-digital converters, transistors, logic gates, multiplexers, and decoders.

Course Competencies

Upon undertaking this course, the student is expected to have a wide range knowledge of different types of analogue and digital electronics components, their distinguishing physical features and structures, and areas of applications. The student is also expected to have a good understanding of the behavior of the components under special circuit conditions, and also be able to identify early signs of component malfunction through measurements and analysis. Additionally, the student is expected to develop basic competence in the use of simulation and modeling tools like Simulink, Proteus VSM, PSpice, and Circuit Maker for the design and simulation of analogue, digital, and mixed electronic (analogue and digital) circuits, and rapid prototyping tools like Very High Speed Integrated Circuit Hardware Description Language (VHDL) for the rapid prototyping and Synthesis of digital electronic circuits.

Course Objectives

The objectives of the course is revised and boldly divided into three sections-objectives for analog electronics, objectives for digital electronics, and objectives for modeling and simulations. The revision of the objectives and the addition of new ones are harmonized and presented as follows:

a. Course Objectives – Analog Electronics

i. Identity different types of transistors, capacitors, and inductors from the perspective of their circuit symbols, and configurations.
ii. Perform a detailed survey of the mathematical equations that govern the operation of important analog devices like transistors, capacitors, and inductors.
iii. Perform in-circuit application and analysis of transistors, capacitors, and inductors
iv. Identify different fundamental types of operational amplifier (op-amp) circuits which includes but not limited to voltage follower, inverting op-amp, non-inverting summing amplifier, differential amplifier, and integrator.
v. Perform a detailed survey of the mathematical equations that govern the operation of different op-amp circuit configurations.
vi. Perform in-circuit application and analysis of different op-amp circuits.

vii. Understand the design and analysis of DC power supply, voltage regulator circuits and analog-to-digital converters.

b. Course Objectives – Digital Electronics

i. Perform a detailed mathematical survey of Boolean algebra and its application digital circuits.
ii. Identify different types of logic gates like XOR, AND, OR, NOT, NAND from the perspective of circuit symbols and governing truth tables.
iii. Understand Karnaugh maps and their applications in digital circuit minimization.
iv. Identify different types of combinational circuits like decoders, multiplexers, encoders, adders, subtractors, multipliers, and demultiplexers from the perspective of circuit symbols and governing truth tables.
v. Identify and understand the difference between types of sequential circuits i.e. asynchronous and synchronous sequential circuits.
vi. Identify different types of sequential circuits like counters, flip-flops, and registers from the perspective of circuit symbols and governing truth tables.

Working Through this Course

A thorough and excellent understanding of this course can be achieved through a systematic and methodic understanding of the contents that will move the reader from the basic to the advanced contents of the course. Further steps that will reinforce the understanding of the course is the study of the network of your organization or proposing one if there is none in existence and be committed to learning and implementing your knowledge.

The approximate duration of the course is 22 weeks under the assumption that the student gives undivided attention to the studies and commits to doing the exercises in the tutor-marked assignments that is expected to be submitted to the tutors

Study Units

There are 12 study units in this course

Module 1

Unit 1 Bipolar Junction Transistors
Unit 2 Small Signal Amplifiers
Unit 3 Field Effect Transistor

Module 2

Unit 1 Operational amplifiers – Types, and Configurations
Unit 2 Mathematical characterization of the functional behavior of op amps.

Module 3

Unit 1	Boolean algebra
Unit 2	Logic gates – Types, circuits symbols, and truth tables
Unit 3	Karnaugh maps and logic circuit simplification
Unit 4	Combinational circuits – Arithmetic & Logic functions: Adders, Subtractors, Comparators
Unit 5	Combinational circuits – Data transmission: Multiplexers, Demultiplexers, Decoders, Encoders

Module 4

Unit 1	Sequential circuits – Synchronous: flip-flops, registers, counters
Unit 2	Sequential circuits – Asynchronous: Asynchronous: analysis procedure, race conditions, stability considerations

References and Further Readings

References for Analog Electronics

Gray, P. R., Hurst, P. J., Lewis, S. H. (2009). Analysis and Design of Analog Integrated Circuits. 5th Ed. *Wiley*. ISBN: 978-0470245996

Dobkin, B., Williams, J. (2011). Analog Circuit Design: A Tutorial Guide to Applications and Solutions. *Newness*. ISBN: 978-0123851857

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Pease, R. (2008). Analog Circuits: World Class Designs. *Newness*. ISBN: 978-0750686273

Fiore, J. (2016). Operational Amplifiers & Linear Integrated Circuits: Theory and Applications. *Independently Published*. ISBN: 978-1796856897

Huijsing, J. (2017). Operational Amplifiers: Theory and Design. 3rd Ed. *Springer*. ISBN: 978-3319281261

Franco, S. (2016). Design with Operational Amplifiers and Analog Integrated Circuits. 4th Ed. *Mc Graw Hill India*. ISBN: 978-9352601943

References for Digital Electronics

Tokheim, R. L., Hoppe, P. E. (2021). Digital Electronics: Principles & Applications. 9th Ed. *Mc Graw Hill Education.* ISBN: 978-1260597868

Kleitz, W. (2011). Digital Electronics: A Practical Approach with VHDL. 9th Ed. *Pearson*. 978-0132543033

Ward, H. H. (2023). Mastering Digital Electronics. *Apress*. ISBN: 978-1484298800

Maini, A. K. (2007). Digital Electronics: Principles, Devices, and Applications. *Wiley*. ISBN: 978-0470032145

Anand, R. (2021). Digital Electronics: Digital Logic Design. *Khanna Book Publishing*

Whitesitt, J. E. (2010). Boolean Algebra and Its Applications. *Dover Publications*. ISBN: 978-0486477671

Gooroochurn, M. K. (2018). Introduction to Digital Logic and Boolean Algebra. *Independently Published*. ISBN: 978-1728793610

Presentation Schedule

The presentation schedule is characterized by important dates on which tutor marked assignments are to be completed and submitted. Adhering to the due dates is absolutely tangential for increasing a good understanding of the course and having time to address areas of weakness perceived from the submitted assignments.

The presentation schedule is included in the course materials.

Assessment

The assessment of this course is divided into two sections- tutor marked assignments, and written examination. In attempting the assignments, the candidate is kindly reminded that the knowledge gained during the course is absolutely tangential to a successful attempt. Consequently, candidates are strongly advised to take very seriously every aspect of the course as the assignments will make 30% of the grading of the course. Sequel to this, a written three-hour examination which makes 70% of the grading of the course will be administered. The examination shall be culled from the course materials and where appropriate, the tutor marked assignments.

Tutor-Marked Assignment

The tutor marked assignment section of the course shall be comprised of sixteen (16) assignments that shall be expected to be submitted for marking.

The total marks for the best four (4) assignments will be 30% of your total course mark.

Assignment questions for the units in this course are contained in the Assignment File. You should be able to complete your assignments from the information and materials contained in your set textbooks, reading and study units. However, you may wish to use other references
to broaden your viewpoint and provide a deeper understanding of the subject.

When you have completed each assignment, send it together with form to your tutor. Make sure that each assignment reaches your tutor on or before the deadline given. If, however, you cannot complete your work on time, contact your tutor before the assignment is done to discuss the possibility of an extension.

Examination and Grading

The final examination for the course shall carry 70% of the total marks available for the grading of this course. The examination will cover all aspects of the course; the candidate is therefore advised to revise all corrected assignments before the examination.

This course endows you with the status of a teacher and that of a learner. This means that you teach yourself and that you learn, as your learning capabilities would allow. It also means that you are in a better position to determine and to ascertain the what, the how, and the when of your course learning. No teacher imposes any method of leaning on you. The course units are similarly designed with the introduction following the table of contents, then a set of objectives and then the concepts and so on.

The objectives guide you as you go through the units to ascertain your knowledge of the required terms and expressions.

Course Marking Scheme

This table shows the break down of marks allocation for the course.

Assessment	**Marks**
Assignment 1 – 4	Best three out of four assignments to count for 30% of course marks
Final Examination	70% of overall course marks
Total	100% of course marks

Table 1: Course marking scheme

Course Overview

After a review of the course overview, it was observed that there is the absence of a structured an systemic approach to the course that progressively enables the student develop higher understanding of each module as progress is made from one unit to another in the module. It was also observed the course overview does not equip the students with the ability to establish the

nexus between theoretical understanding of a unit in a module and the application of the unit in electronic designs via in-circuit applications. It is against this backdrop that the course overview has been reviewed an presented as follows.

Unit	Title of Work	Week(s) Number	End of Unit Assessment
	Course guide	1	
Module 1			
1	Bipolar Junction Transistors	1 - 2	
4	Small Signal Amplifiers	3	Assignment 1
5	Field Effect Transistors	4	Assignment 2
Module 2			
1	Operational amplifiers – Types, and Configurations	5	Assignment 3
2	Mathematical characterization of the functional behavior of op amps.	6	Assignment 4
Module 3			
1	Boolean algebra	8	Assignment 6
2	Logic gates – Types, circuits symbols, and truth tables	9	Assignment 7
3	Karnaugh maps and logic circuit simplification		
4	Combinational circuits – Arithmetic & Logic functions: Adders, Subtractors, Comparators	10 - 11	Assignment 8
5	Combinational circuits – Data transmission: Multiplexers, Demultiplexers, Decoders, Encoders	12 - 13	Assignment 9
Module 4			
1	Sequential circuits – Synchronous: flip-flops, registers, counters	14 - 15	Assignment 10
2	Sequential circuits – Asynchronous: analysis procedure, race conditions, stability considerations	16 - 17	Assignment 11
Revision		18	
Examination		19	
Total		22 weeks	

How to get the Most from the Course

In distance learning the study units replace the university lecturer. This is one of the great advantages of distance learning; you can read and work through specially designed study materials at your own pace, and at a time and place that suit you best. Think of it as reading the lecture instead of listening to a lecturer. In the same way that a lecturer might set you some reading to do, the study units tell you when to read your set books or other material. Just as a lecturer might give you an in-class exercise, your study units provide exercises for you to do at appropriate points.

Each of the study units follows a common format. The first item is an introduction to the subject matter of the unit and how a particular unit is integrated with the other units and the course as a whole. Next is a set of learning objectives. These objectives enable you know what you should be able to do by the time you have completed the unit. You should use these

objectives to guide your study. When you have finished the units you must go back and check whether you have achieved the objectives. If you make a habit of doing this you will significantly improve your chances of passing the course. Remember that your tutor's job is to assist you. When you need help, don't hesitate to call and ask your tutor to provide it.

i. Read this Course Guide thoroughly.
ii. Organize a study schedule. Refer to the 'Course Overview' for more details. Note the time you are expected to spend on each unit and how the assignments relate to the units. Whatever method you chose to use, you should decide on it and write in your own dates for working on each unit.
iii. Once you have created your own study schedule, do everything you can to stick to it. The major reason that students fail is that they lag behind in their course work.
iv. Turn to Unit 1 and read the introduction and the objectives for the unit.
v. Assemble the study materials. Information about what you need for a unit is given in the 'Overview' at the beginning of each unit. You will almost always need both the study unit you are working on and one of your set of books on your desk at the same time.
vi. Work through the unit. The content of the unit itself has been arranged to provide a sequence for you to follow. As you work through the unit you will be instructed to read sections from your set books or other articles. Use the unit to guide your reading
vii. Review the objectives for each study unit to confirm that you have achieved them. If you feel unsure about any of the objectives, review the study material or consult your tutor.
viii. When you are confident that you have achieved a unit's objectives, you can then start on the next unit. Proceed unit by unit through the course and try to pace your study so that you keep yourself on schedule.
ix. When you have submitted an assignment to your tutor for marking, do not wait for its return before starting on the next unit. Keep to your schedule. When the assignment is returned, pay particular attention to your tutor's comments, both on the tutor-marked assignment form and also written on the assignment. Consult your tutor as soon as possible if you have any questions or problems.
x. After completing the last unit, review the course and prepare yourself for the final examination. Check that you have achieved the unit objectives (listed at the beginning of each unit) and the course objectives (listed in this Course Guide).

Facilitation

There are 12 hours of tutorials provided in support of this course. You will be notified of the dates, times and location of these tutorials, together with the name and phone number of your tutor, as soon as you are allocated a tutorial group.

Your tutor will mark and comment on your assignments, keep a close watch on your progress and on any difficulties you might encounter and provide

assistance to you during the course. You must mail or submit your tutor-marked assignments to your tutor well before the due date (at least two working days are required). They will be marked by your tutor and returned to you as soon as possible.

Do not hesitate to contact your tutor by telephone, or e-mail if you need help. The following might be circumstances in which you would find help necessary. Contact your tutor if:

- you do not understand any part of the study units or the assigned readings,
- you have difficulty with the self-tests or exercises,
- you have a question or problem with an assignment, with your tutor's comments on an assignment or with the grading of an assignment.

You should try your best to attend the tutorials. This is the only chance to have face-to-face contact with your tutor and to ask questions which are answered instantly. You can raise any problem encountered in the course of your study. To gain the maximum benefit from course
tutorials, prepare a question list before attending them. You will learn a lot from participating in discussions actively.

Ice Breaker

Students are to write what they know about analogue and digital electronics, and what they also expect from the course.

MAIN COURSE

CONTENTS

MODULE 1

Unit 1 Bipolar Junction Transistors
Unit 2 Small Signal Amplifiers
Unit 3 Field Effect Transistors

UNIT 1 BIPOLAR JUNCTION TRANSISTORS

CONTENTS

1.0 INTRODUCTION

A transistor is a three-terminal semiconductor device that can be used for amplification and switching. Amplification consists of magnifying a signal by transferring energy to it from an external source; whereas a transistor switch is a device for controlling a relatively large current between or voltage across two terminals by means of a small control current or voltage applied at a third terminal. There are two major families of transistors are bipolar junction transistors, or BJTs; and field-effect transistors, or FETs. As will be shown, the BJT acts essentially as a current-controlled device, while the FET behaves as a voltage-controlled device.

2.0 OBJECTIVES

At the end of this unit, students should be able to:

- be able to IDENTIFY basic transistor amplifier topologies
- be able to ANALYZE basic amplifier topologies for gains and resistances
- be able to DISCUSS the relative properties of various amplifier topologies

- be able to DESIGN basic amplifiers to meet or exceed stated specifications.

3.0 MAIN CONTENT

The Bipolar Junction Transistor (BJT)
The pn junction forms the basis of a large number of semiconductor devices. A BJT is formed by joining three sections of semiconductor material, each with a different doping concentration. The three sections can be either a thin nregion sandwiched between p+ and p layers, or a p region between n and n+ layers, where the superscript “plus” indicates more heavily doped material. The resulting BJTs are called pnp and npn transistors, respectively:

The figure 1.1 below shows the block diagrams and circuit symbols of both the npn ad the pnp transistors.

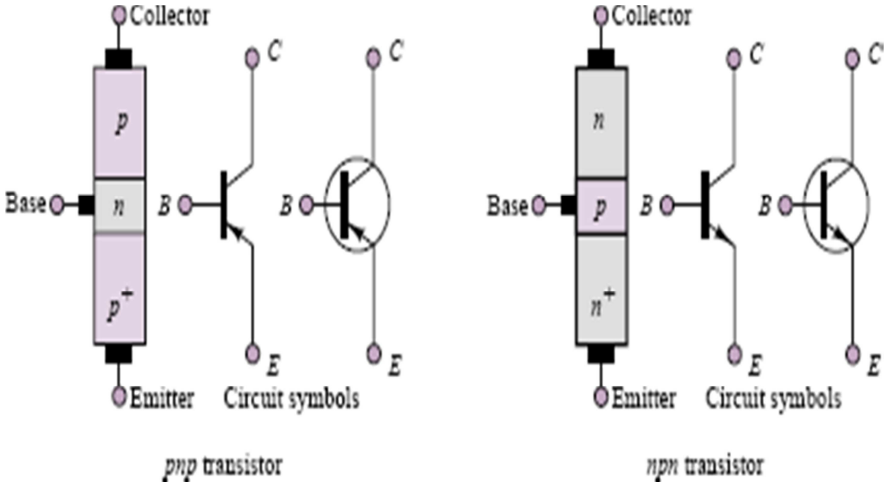


Figure 1.1 transistor symbols

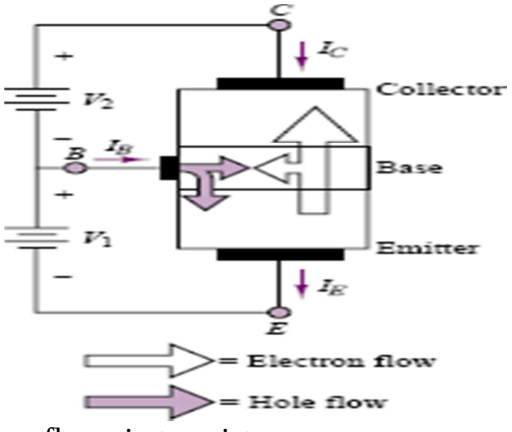


Figure 1.2 electron flows in transistors

The operation of the npn BJT can be explained by considering the transistor as consisting of two back-to-back pn junctions. The base-emitter (BE) junction acts very much like a diode when it is forward-biased; thus, the corresponding flow of hole and electron currents from base to emitter when the collector is open and the BE junction is forward-biased, is shown in figure 1.2.Note that the electron current has been shown larger than the hole current, because of the heavier doping of the n side of the junction. Some of the electron-hole pairs in the base will recombine; the remaining charge carriers will give rise to a net flow of current from base to emitter. It is also important to observe that the base is much narrower than the emitter section of the transistor.

The flow of electrons in the transistor is represented by the equation below.

IE = IB + IC 1

Since the transistor is biased in the active region a small base current controls the much larger collector current.

where IC = βIB 2

where β is a current amplification factor dependent on the physical properties of the transistor. Typical values of β range from 20 to 200. The operation of a pnp transistor is completely similar to that of the npn device, with the roles of the charge carriers (and therefore the signs of the currents) reversed.

I E □

I E □

IB □

(1 □

□ I B 3

□)IB 4

from the equation (4) above

$$I_B = \frac{I_E}{(1+\beta)} \quad \text{.....5}$$

$$I_C = \left(\frac{\beta}{1+\beta}\right) I_E \quad \text{.....6}$$

Equation 6 can be written as

Thus $\alpha = \left(\frac{\beta}{1+\beta}\right)$ where α = common base gain

IC □

□ IE

Bipolar Junction Transistor Configurations

Transistors can be configured in three different modes with one pair of terminals for the input and another pair for the output. These configurations are:

Common emitter
Common collector
Common base.
Common Emitter
In the common emitter configuration, the input terminal is the base while the output terminal is the collector and the emitter is common to both the input and the output as shown in figure 1.3 below.

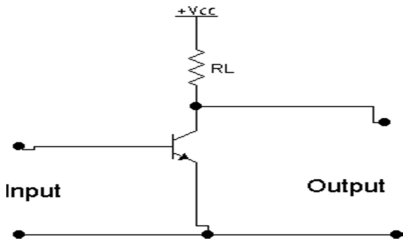


Figure 1.3 Common Emitter configurations

α

The current gain for this configuration is given by
output _ current IC
input _ current IB

Common Collector

In the common collector configuration, the input terminal is the base while the output terminal is the emitter and the collector is common to both the input and the output as shown in figure 3.4 below.

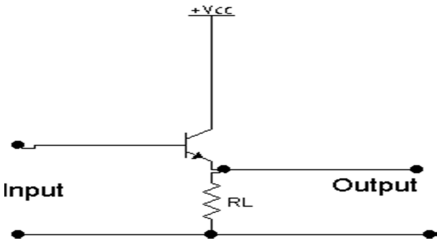


Figure 1.4 Common collector configurations

I E
The current gain for this configuration is given by
B
Common Base
In the common base configuration, the input terminal is the emitter while the output terminal is the collector and the base is common to both the input and the output as shown in figure 1.5 below

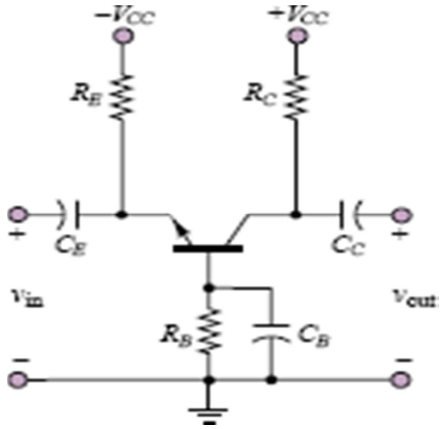


Figure 1.5 common base configuration

IC
The current gain for this configuration is given by $\overline{I}$
E

The gain for the CB configuration is always less than 1, so the CB configuration is not used for current amplification .The CC and CE configurations both have a high gain but the input impedance of the CE configuration is higher than that of the CC. This makes the CE configuration the preferred choice for amplifiers in circuit design.

Loads Lines

The load line is a line drawn based on the DC operating characteristics of the circuit. It enables the visualization of the transistor characteristics. It is determined by using the DC equations of the circuit. The Ic (max) and Vce (max) are used to determine the end points of the line, these points are then joined together and superimposed on the transistor characteristics.

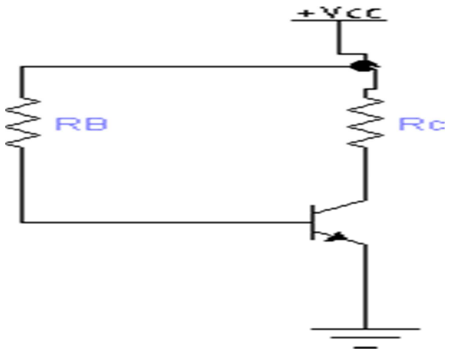


Figure 1.6 Amplifier circuit

From the circuit 1.6, the analysis is done below From the output equation
Vcc □ ICRC □ VCE

The load line is determined by identifying the two endpoints of the line. The are determined by assuming VCE = 0 and finding Ic, and the V subscribe is determined by assuming Ic= 0.

From the output equation, with Ic = 0, Vcc = VCE
With VCE = 0 Vcc = IcRc
Ic(max) = Vcc
Rc

The load line is sketched in the figure 1.7 below

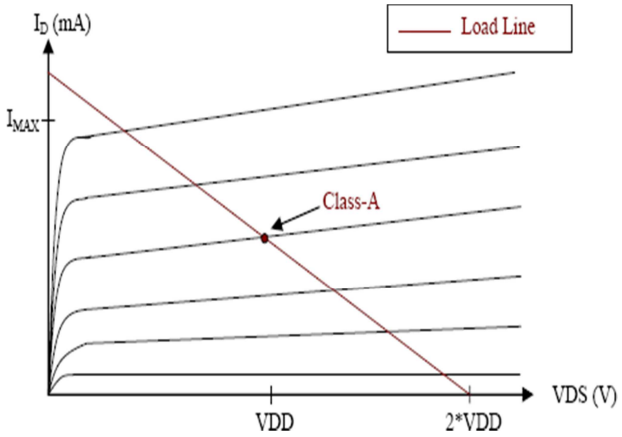


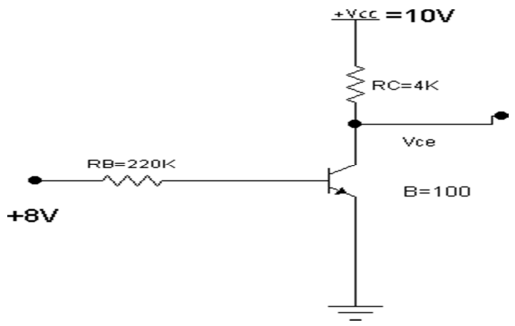
Figure 1.7 load line

The curves are generated at different base currents. The Q point (operating Point) is the intersection of the Ic and the Vce on the load line for any particular base current.

From the graphs, as Ic rises from 0, the mode of operation of the transistor changes from cutoff to active and when the Ic gets to the maximum, the transistor gets to the saturation region of operation.

Example 1

Given the circuit below, determine the load line.



From the output equation

Vcc □ ICRC □ VCE

With Vce = 0

Ic(max) =
10 □ ___
4K

2.5mA

With Ic = 0

Vce = 10V

Bipolar Junction Transistor Biasing

The transistor can serve either as a switch or an amplifier. The mode of operation of each transistor is determined by the bias condition in which it operates.

Biasing can be defined as the setting up of the DC voltages and current in an electronic circuit.

From the output characteristics, the transistor has 3 regions of operation.

Saturation region
Active region
Cutoff region

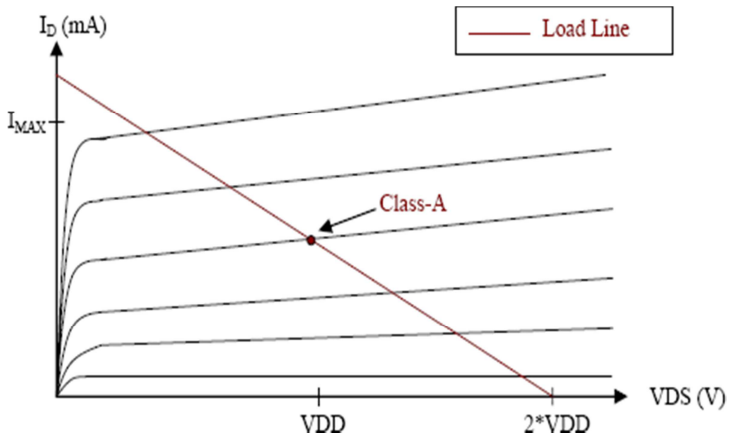
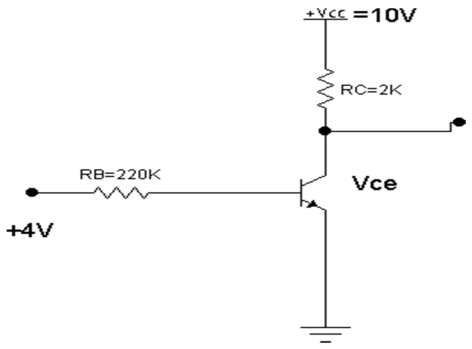


Figure 1.8 Q-point

The Q point or dc operating point is that point on the load line where the Icq and Vceq intercept on the load line. The transistor when operating as a switch is biased in the saturation or cutoff region but for the transistor to be used as an amplifier it is biased in the active region. With transistor in the forward active region the voltage across the B-E junction is V subscribe (on) is 0.7V for silicon transistors and 0.4V for germanium transistors.

The determination of the q point is through the process of biasing.
Example 2

Calculate the base, collector and emitter currents for the circuit shown below.
β =200



From the output equation Vcc = IcRc + VCE
From the input equation

VBB= IBRB + VBE

I = VBB □ VBE □
RB
4 □ 0.7 □ 15□ A
220K
Ic = βIB = (200)(15μA) = 3mA

IE = (1+β).
IB = (200+1) (15μA) = 3.02mA
VCE = Vcc – IcRc = 10 – (3mA)(2K) = 4V

Types Common Emitter Biasing

There are different types of bias circuit with each having its advantages and disadvantages.

1. Base Bias

This is the simplest type and is also known as fixed bias. The quiescent base current is established by a single base resistor as shown in figure 1.9 below.

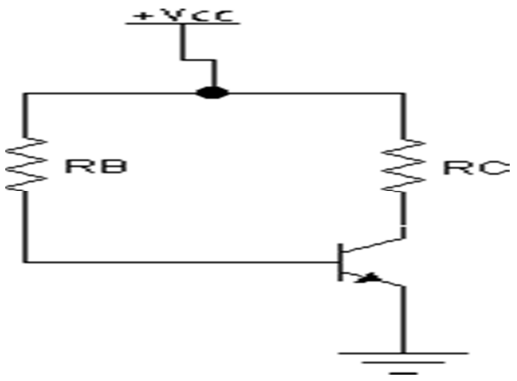


Figure 1.9 base bias

Biasing of this circuit will involve the selection of appropriate values for the base resistance and collector resistance.

Analysis

Input equation

Vcc □ IBRB □ VBE (1)
IBRB □

IBQ □

VCC □ VBE

VCC □ VBE
RB
(2)

(3)
RB □
VCC □ VBE IBQ
(4)

This equation yields the Quiescent base current IBQ

From the circuit, the output equation is derived below

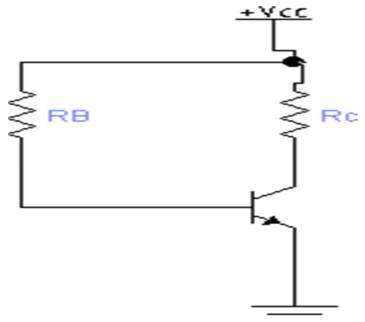
Vcc □

ICRC □ VCE
(5)
ICQRC □
VCC □ VCE (6)
ICQ □
RC □
VCC □ VCE RC
VCC □ VCE
ICQ

(7)
(8)

Example 3

Given the circuit below, design the amplifier for the following specifications:



VCC = 12V, β = 100, Vbe = 0.7, Icq = 1mA Vceq = 6V
Solution

From the input equation,
VCC □

IBRB □
IBRB □
IBRB □ VBE

VCC □ VBE □
II .3V

12 □
0.7
From the output equation
Vcc □
IcRc □

IcRc □ Vce Vcc □ Vce □

12 □ 6
12 □ 6
Ic □ ——
Icq □
~~IBQ~~
1mA
□
□ 6K□
□ IBQ □
Icq □ ___
□
1mA □ ___
100 10□ A

The base resistance is determined from the input equation to be

IBQRB □ VCC □ Vbe(on)
12 □ 0.7
RB □~~10□ A~~
□ 1.13M□

$$Vcc = IcRc + Vce$$
$$Ic = 0,$$

$$Vce = Vcc = 12V$$
$$Vce = 0$$

$$Ic = \frac{Vcc}{Rc} = \frac{12}{6K} = 2mA$$

The load line is determined to be

From the various formulas used above, the Icq is dependent to a large extent on the β. The beta (β) varies with temperature so any circuit built with too much dependence on β will be very unstable.

Base Bias with Collector Feedback

The base is connected to the collector as shown in the circuit in figure 1.10 below

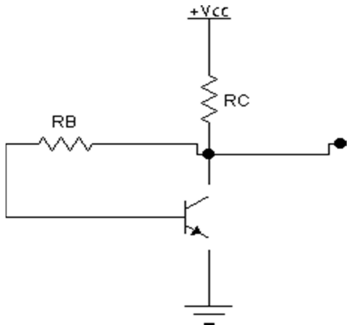


Figure 1.10 Base bias with collector feedback

Output equation

VCC □
(IC □
I B)RC □ VCE 1

The collector current and the base currents flow through the collector resistor

But IC >> IB

IC(sat) = Vcc
Rc
Since there is no emitter resistor the out put equation becomes

VCC □
(IC □
I B)RC □ VC
VC □ Vcc □
(IC □
I B)RC

Since Vc also forms part of the input equation, the input equation becomes:

$$V_C = I_B R_B + V_{BE}$$

$$Vcc - (I_C + I_B)R_C = I_B R_B + V_{BE}$$

Since $I_C >> I_B$

$$Vcc - I_C R_C = I_B R_B + V_{BE}$$

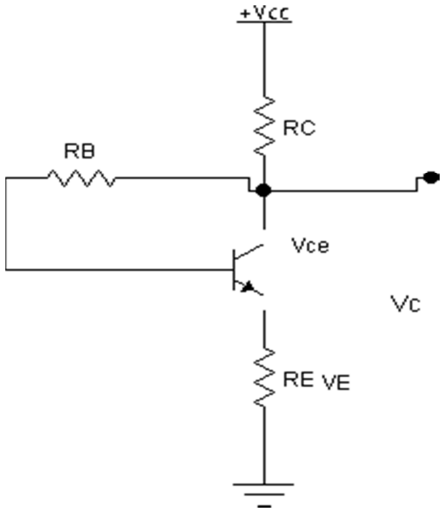
But $I_B = \frac{I_C}{\beta}$

$$\frac{I_C R_B}{\beta} + V_{BE} = Vcc - I_C R_C$$

The collector current can be derived from the expression below.

Vcc □ VBE
Ic □ ————
RB □ Rc
□
□ I E

From the expression for collector current, the effect of the transistor gain on the collector current is reduced leading to better system stability.



Base Bias with Collector and Emitter Feedback

Figure 1.11 Base Bias with collector and emitter feedback

From the output equation:

$$V_{CC} = (I_C + I_B)R_C + V_{CE} + I_E R_E$$

$I_C >> I_B$ and $I_C = I_E$

$$V_{CC} = I_C R_C + V_{CE} + I_C R_E = V_{CE} + I_C(R_C + R_E)$$

$$I_C = \frac{V_{CC} - V_{CE}}{(R_E + R_C)}$$

At saturation (VCE =0)

I □ VCC

C (R □ R)
C

The actual value of Ic is derived using the input equation since in most cases the VCE is unknown

From the input equation

VCC □
IC RC □ VBE □
I B RB □ I E RE
Since IC = IE

$$V_{CC} = I_C R_C + V_{BE} + I_B R_B + I_C R_E$$

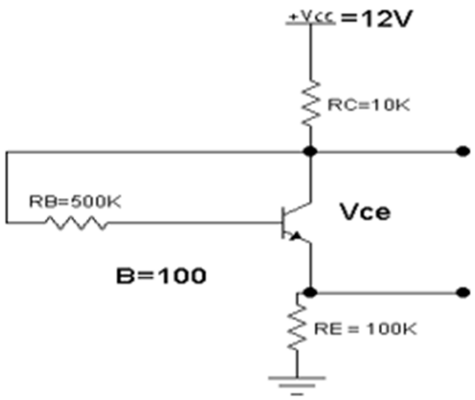
$$V_{CC} - V_{BE} = I_C(R_C + R_E) + I_B R_B$$

But $I_B = \frac{I_C}{\beta}$

$$V_{CC} - V_{BE} = I_C(R_C + R_E) + \frac{R_B}{\beta}$$

$$I_C = \frac{V_{CC} - V_{BE}}{(R_E + R_C + \frac{R_B}{\beta})}$$

Example 4
Determine the Ic(sat),VCE and Vc. In the circuit below. Neglect VBE



From the output equation:

$$V_{CC} = (I_C + I_B)R_C + V_{CE} + I_E R_E$$

$I_C >> I_B$ and $I_C = I_E$

$$V_{CC} = I_C R_C + V_{CE} + I_C R_E = V_{CE} + I_C (R_C + R_E)$$

$$I_C = \frac{V_{CC} - V_{CE}}{(R_E + R_C)}$$

At saturation (VCE =0)

$$I_c(sat) = \frac{12}{(100K + 10K)} = 0.11mA$$

$V_C = V_{CE} + V_E$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

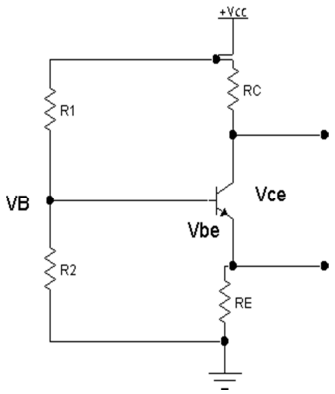
$V_E = I_E R_E$

To determine IC we use the input equation
VCC □
IC RC □ VBE □
I B RB □
I E RE

Since IC = IE

VCC □
IC RC □ VBE □
I B RB □
IC RE
VCC □ VBE □
IC (RC □
RE) □
I B RB
But

VCC
I B □
VBE



IC

□ IC
(RC □

RE) □ B *R*
□

I □ VCC □ VBE

C RB

(RE □ RC □ □)

I □ 12 □ 12

C
(10k □ 100k □ 500k)
100
115k =0.1mA

Substituting the value of IC in the equation for VCE we have

VCE □ VCC □
IC (RC □
RE) □ 12 □
0.1mA(110K) □ 1V

VC = VCE + VE =1 +ICRE = 1 + 0.1mA(100K) =11V
Voltage Divider Bias

From the circuit diagram in figure 1.12, the voltage divider bias is analyzed below as follows.
Figure 1.12 Voltage divider bias

From the potential (voltage) divider equation
VB □
Vcc * R2

R1 □ R2

VB = Vbe + VE

VE = VB – Vbe but VB >>Vbe
IE =
VE □
RE
VB □ Vbe □ VB RE RE
From the output equation

VCC □
IC RC □ VCE □
I E RE

VC = VCE + VE
VCE □ VCC □
IC (RE □
RC)

With VCE = 0 in the output equation, Ic is determined as

Vcc
IC(sat) =
E RC

The base voltage is set by the resistors R1 and R2 thus the effect of the transistor forward gain is reduced .The D.C bias is independent of β.

4.0 CONCLUSION

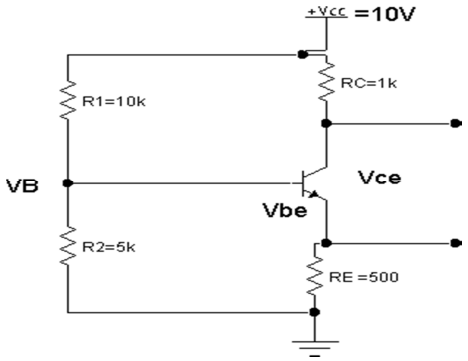
In this unit you have been introduced to the transistor amplifier and the different types of biasing arrangements and transistor configurations.

5.0 SUMMARY

In this unit we have been able to extend knowledge of the theory and applications of transistors and transistor amplifier design.

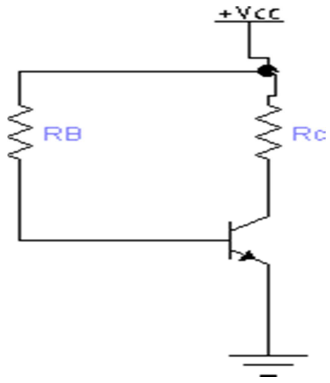
6.0 TUTOR-MARKED ASSIGNMENT

Determine the VCE and IC in the circuit diagram shown below. Vbe = 0.7



2. Given the circuit below, design the amplifier for the following specifications:

VCC = 12V, β = 100, Vbe = 0.7, Icq = 1mA Vceq = 6V



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McGraw-Hill Publishers.

UNIT 2 SMALL SIGNAL AMPLIFIERS

CONTENTS

1.0 INTRODUCTION

Electronic amplifying devices such as BJT and FET have three terminals (E,B,C and S, G,D). In a basic amplifying circuit, one of the terminals is made common while the other two serve as input and output ports. Small-signal models for the BJT take advantage of the relative linearity of the base and collector curves in the vicinity of an operating point. These linear circuit models work very effectively, providing that the transistor voltages and currents remain within some region around the operating point. This condition is usually satisfied in small-signal amplifiers used to magnify low-level signals (e.g., sensor signals). For the purpose of our discussion, we use the hybrid-parameter (h-parameter) small-signal model of the BJT, to be discussed presently. Note that a small-signal model assumes that the DC bias point (Q-point) of the transistor has been established. The following convention will be used: each voltage and current is assumed to be the superposition of a DC component (the quiescent voltage or current) and a small-signal AC component. The former is denoted by an uppercase letter and the latter by an uppercase letter preceded by the symbol Δ. Thus,

$iB = IBQ + \Delta IB \quad iC = ICQ + \Delta IC$
$vCE = VCEQ + \Delta VCE$

2.0 OBJECTIVES

At the end of this unit, student should be able to:

- be able to IDENTIFY the transistor hybrid parameters
- be able to ANALYZE amplifier topologies for gains and impedances
- be able to DISCUSS the relative properties of various amplifier configurations
- be able to DESIGN basic amplifiers to meet or exceed stated specifications.

3.0 MAIN CONTENT

Transistor Hybrid parameters

The Hybrid parameters are specifications used in the analysis of transistor amplifiers there are four h parameters and these are:

The parameter hie which is approximately equal to the ratio Δ VBE/ ΔIB. Physically, this parameter represents the forward resistance of the BE junction.

The parameter hre which is representative of the fact that the IB- VBE curve is slightly dependent on the actual value of the collector- emitter voltage, VCE. However, this effect is virtually negligible in any applications of interest to us. Thus, we shall assume that hre ≈ 0. A typical value of hre for VCE ≥ 1 V is around 10-2.

The parameter hf e is the current ratio Δ IC /ΔIB. This parameter represents the current gain of the transistor and is approximately equivalent to the parameter β introduced earlier. For the purpose of our discussion, β and hf e will be interchangeable, although they are not exactly identical.

The parameter hoe may be calculated as hoe = ΔIC/ Δ VCE From the collector characteristic curves. This parameter is a physical indication of the fact that the IC-VCE curves in the linear active region are not exactly flat; hoe represents the upward slope of these curves and therefore has units of conductance (S). Typical values of hoe are around 10-5 S. this parameter is often assumed to be negligible.

$$h_{ie} = \left.\frac{\partial v_{BE}}{\partial i_B}\right|_{I_{BQ}} \quad (\Omega)$$

$$h_{oe} = \left.\frac{\partial i_C}{\partial v_{CE}}\right|_{V_{CEQ}} \quad (\mathrm{S})$$

$$h_{fe} = \left.\frac{\partial i_C}{\partial i_B}\right|_{I_{BQ}} \quad \left(\frac{\mathrm{A}}{\mathrm{A}}\right)$$

$$h_{re} = \left.\frac{\partial v_{BE}}{\partial v_{CE}}\right|_{V_{CEQ}} \quad \left(\frac{\mathrm{V}}{\mathrm{V}}\right)$$

Analysis of a Single Stage Transistor Amplifier Small Signal Operation

In order to fully analyze a transistor amplifier, the analysis is broken into AC and DC analysis. In the DC analysis all capacitors are regarded as open circuits, while for the AC analysis, the capacitors are regarded as short circuits and the DC source is replaced by a ground.

The purpose of the analysis is to determine the different specifications of the circuit. These specifications include the input impedance, output impedance and the circuit gain.

Example 1

Given the circuit below, determine the Q point voltage and current values and AC open-loop voltage gain of the amplifier of Figure 2.1; the amplifier employs a 2N5088 npn transistor. β=350

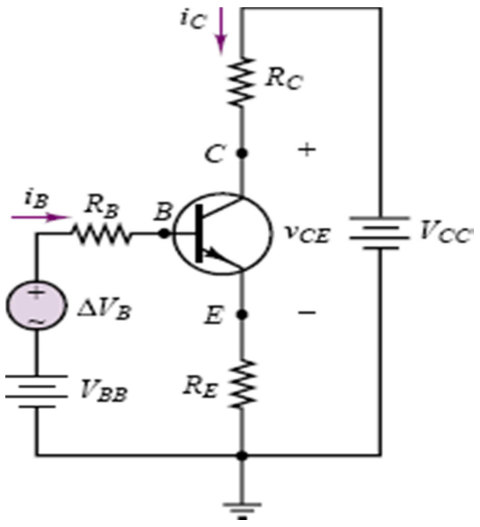


Figure 2.1

Analysis

Q-point calculation

We first write the collector circuit equation by applying KVL:

VCC = VCE + RCIC + REIE = VCE + RCIC + RE(IB + IC)

≈ VCE + (RC + RE)IC

where the emitter current has been approximately set equal to the collector current since the current gain is large and IC >> IB.

Next, we write the base circuit equation, also via KVL:

VBB = RBIB + VBE + REIE = (RB + (β + 1)RE)IB + Vbe

The above equation can be solved numerically (with hf e = β) to obtain:

$$I_B = \frac{V_{BB} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{6 - 0.6}{100 \times 10^3 + 351 \times 100} = 40\mu A$$

Then,

IC = βIB = 350 X 40 x 10-6 = 14 mA

and

VCE = VCC − (RC + RE)IC = 12 − 600 x 40 x 10-3 = 3.6 V

Thus, the Q point for the amplifier is:

IBQ = 40 μA, ICQ = 14 mA and VCEQ = 3.6 V

Confirming that the transistor is indeed in the active region.

From previous discussion, it has been verified that the common emitter configuration is the best for signal amplification. We shall be looking at the single stage common emitter amplifier.

Any amplifier circuit has the following parts:

The Bias Circuit
The Load Circuit
The Coupling Circuit

The bias circuit has been discussed so we focus on the other component parts.

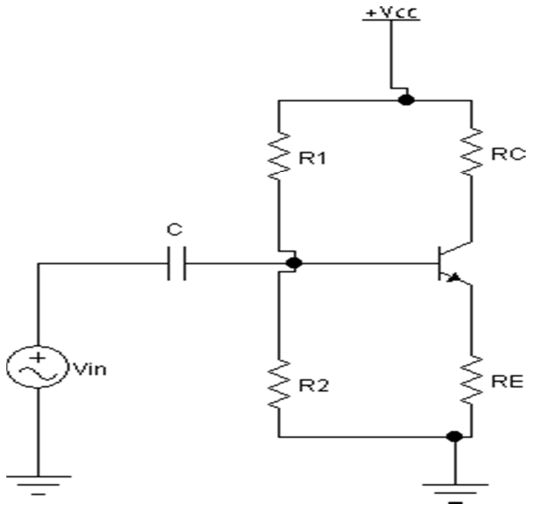


Fig 2.2: CE amplifier circuit

From the diagram above, the following are the responsibility of the different components.

C = Coupling capacitor. it prevents dc signals in the source from upsetting the amplifier's Q point values.

R1 and R2 = potential divider bias resistors
RC = load/collector resistor
RE = Emitter resistor

Given a common emitter amplifier circuit, to analyze such a circuit we need to consider its DC and AC characteristics.

Example 2

Given the circuit with the following parameters below, (βdc =150 and βac = 160)

where βdc =DC gain and βac = AC gain. Determine the circuit specifications given the following component parameters. RE = 600Ω Rc = 1kΩ R1 = 22kΩ R2= 4.7kΩ

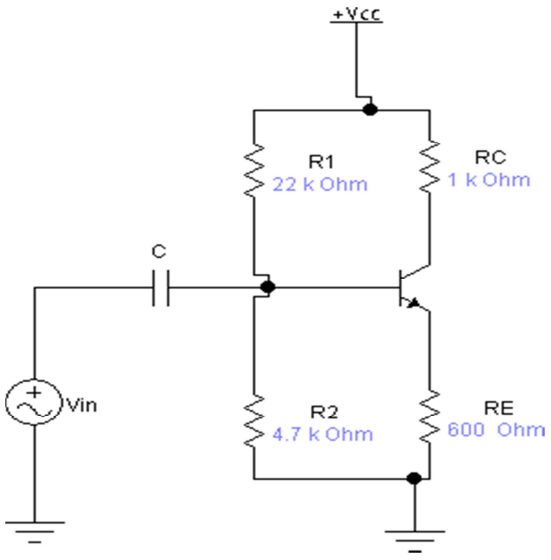


Fig 2.3: CE amplifier circuit

In order to understand the operation of the circuit given above, we will have to perform both the DC and AC analysis.

DC Analysis

Before the DC analysis is performed, all coupling capacitors are regarded as open circuit. This will yield the following representation of the circuit above.

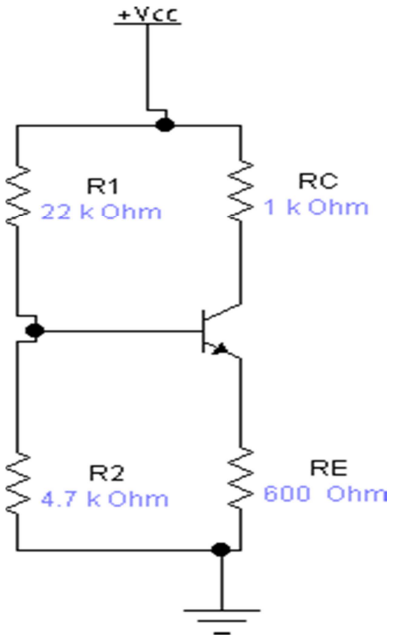


Fig 2.4:

From Ohms Law,

Rin □
Vin Iin

Vin =Vbe + IERE . Vbe = 0.7 for silicon transistor which is the most widely used type. IERE >> Vbe

Vin = IERE

Rin □I E RE

Iin
Vin □
IinRin □
IE RE
but IE □ Ic = βIb . The base current Ib is the input
current and RIN is the resistance at the base so, Iin = Ib and RIN = RB
Vin □
□ IbRE =IbRB

RB □□ IbRE Ib
canceling Ib from both the numerator and denominator we have the DC input resistance RB to be, RB □□ RE

Inserting the values of the components, the Dc input resistance of the circuit is given by

RIN = RB □ □ dcRE =150 x 600 = 90KΩ

Note: If RB is more than 10 times R2 then the voltage divider rules is used VB □ □
R2 □Vcc □ □

4.7k
□ x12 □
2.11V
□ R1 □
R2 □
□ 22k □
4.7k □
VE =VB –Vbe =2.11 – 0.7=1.41V
IE = VE □
RE
1.41 □
600

mA
Since Ic =IE

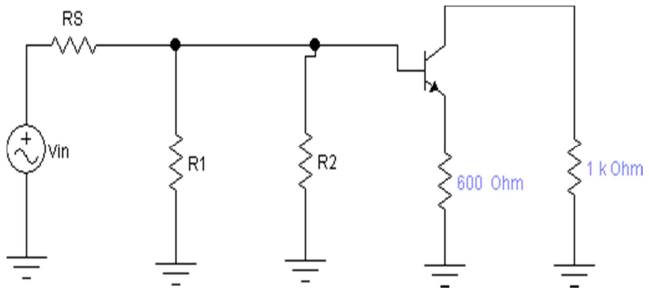
VC = Vcc- IcRC = 12 – 2.4 = 9.6V VCE = VC –VE = 9.6 – 1.41 = 8.19V

AC Analysis

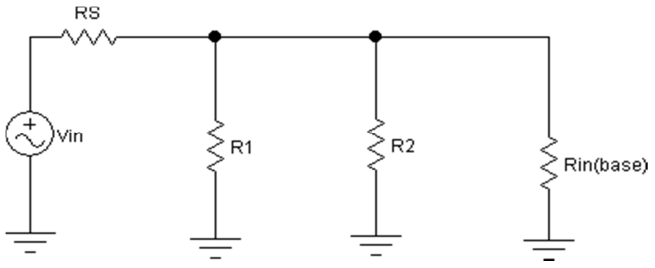
For the ac analysis, the circuit is redrawn with the following assumptions:

All capacitors are short circuit

DC sources are replaced by ground



This circuit is further reduced to the circuit shown below



Rin (base) is the resistance at the base of the transistor and it is derived with the ac emitter resistance added in series to the RE.

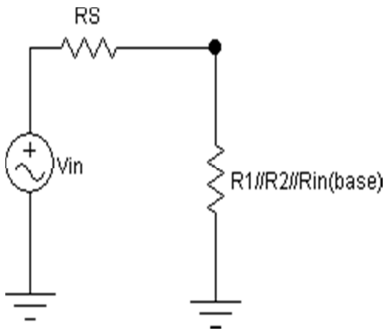
Rin (base) = βac(re + RE)

The ac emitter resistance is given by

$$re = \frac{25mV}{IE}$$

3.3 Input Impedance

The total input impedance of the circuit is the parallel combination of R1 ,R2 and Rin(base).Thus the circuit is reduced to the following:



Input Impedance = R1//R2//Rin(base).

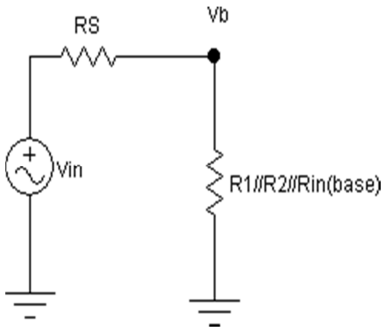
From the component values of the circuit assuming a source impedance of 300Ω, the input impedance is computed to be

Rin(base) = 160(re + 600)
But re 25mV
IE 25mV

mA=10.4Ω

IE is the DC emitter current computed to be 2.4mA. Rin (base) = 160 (10.4 + 600)
Rin(base) =160(610.4) = 97664 Ω

The voltage at the base of the transistor (Vb) is determined below



If RS << Rin(input impedance) then Vb = Vin. If not then the voltage divider equation is used as shown below.

$$Vb = \left(\frac{Rin}{RS + Rin} \right) Vin$$

Compute the input impedance and the voltage at the base of the transistor

Output Impedance

The output resistance looking at the collector is approximately equal to RC. In situations where a load is connected in parallel with the RC, the output resistance will be equal to the parallel combination of both the Rc and the load resistance. Thus a load (RL) connected to the output affects the gain.

RC1=RC//RL

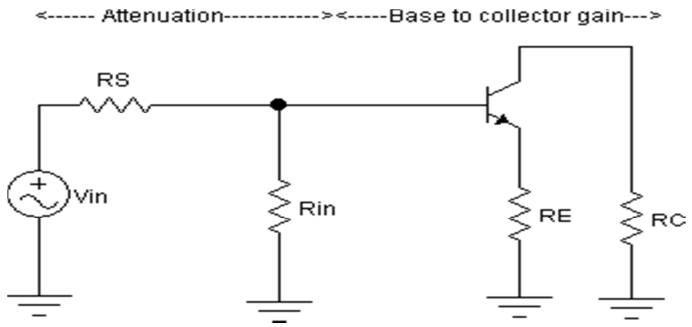
Voltage Gain

The voltage gain is the ratio between the output voltage and the input voltage.

AV □□ Output _ voltage □
□
□
VC □
___
□
Input _ voltage □
IcRC
Vb IE(re □
IERC
RE)
IE(re □
AV □
RE) RC
(re □ RE)
RE)

This is the voltage gain from the base to the collector of the transistor.

The total circuit gain is made up of the attenuation due to the source resistance and the base to collector gain as shown below.



$$Vb = \left(\frac{Rin}{RS + Rin} \right) Vin$$

$$AV^{1} = \frac{RC}{(re + RE)} \left(\frac{Vb}{Vin} \right)$$

Effects of Emitter Bypass Capacitor on the CE Amplifier

When a capacitor is connected across the emitter resistor it bypasses the RE as the capacitor acts as a sort circuit for the AC signals. Thus the Ac voltage gain becomes

AV □
RC

—
(re)

RE is neglected and the gain increases.

This increase in gain however leads to a reduction in gain stability because the re (ac emitter resistance varies with temperature)

4.0 CONCLUSION

In this unit you have been introduced to the small signal operation of the BJT amplifier and the transistor hybrid parameters.

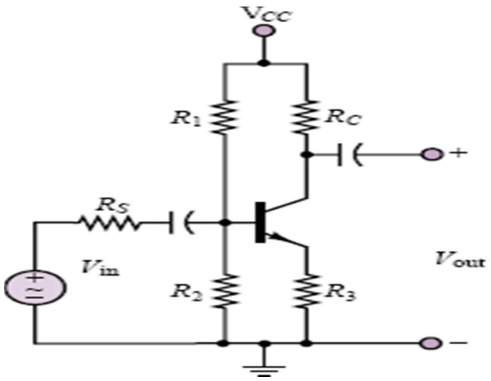
5.0 SUMMARY

In this unit we have been able to extend knowledge of the theory and applications of transistors and small signal transistor amplifier design.

6.0 TUTOR-MARKED ASSIGNMENT

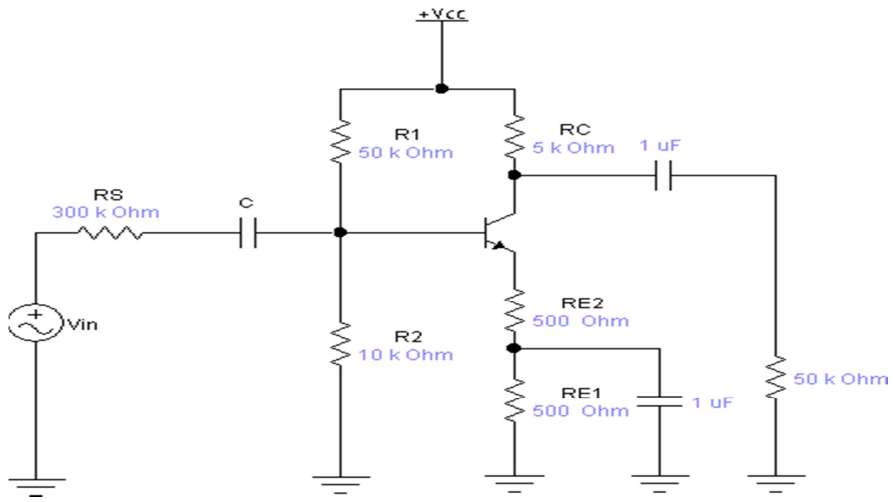
Determine the Q point of the amplifier shown below. Vbe = 0.7 V; β = 100; VCC = 15

V.R1 = 68 k_; R2 = 11.7 k_; RC = 200 _; RE = 200 _.



Given the amplifier circuit below determine the total output voltage (ac and dc).Vcc = 10V, βdc=150, β = 175 RS = 300Ω,R1=50KΩ,R2 = 10KΩ, Rc = 5KΩ,

RE1=RE2 = 500Ω, Load =50KΩ



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UNIT 3 FIELD EFFECT TRANSISTORS

CONTENTS

1.0 INTRODUCTION

The concept upon which the field - effect transistor or FET is based is that the width of a conducting channel in a semiconductor may be varied by the external application of an electric field. Thus, FETs behave as voltage-controlled resistors. These devices can be grouped into three major categories. The first two categories are both types of metal-oxide-semiconductor field-effect transistors,or MOSFETs: enhancement-mode MOSFETs and depletion-mode MOSFETs. The third category consists of junction field-effect transistors, or JFETs. In addition, each of these devices can be fabricated either as an n-channel device or as a p-channel device, where the n or p designation indicates the nature of the doping in the semiconductor channel.

2.0 OBJECTIVES

At the end of this unit, students are expected be able to:

- be able to IDENTIFY field effect transistor symbols
- be able to ANALYZE basic FET amplifier topologies for gains and resistances
- be able to DISCUSS the relative properties of various FET configurations
- be able to DESIGN basic amplifiers to meet or exceed stated specifications.

3.0 MAIN CONTENT

Junction Field Effect Transistors

There are two general classes of FETs

The Metal Oxide Semiconductor FET (MOSFET)
The Junction FET (JFET)

FET Configurations

The FET is similar to the BJT transistor in terms of the number of terminals and configuration. The FET has three terminals as shown below.

G

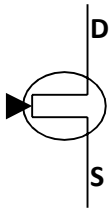
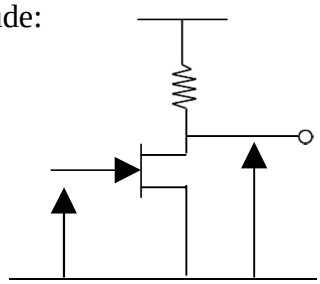


Fig 3.1 FET symbol

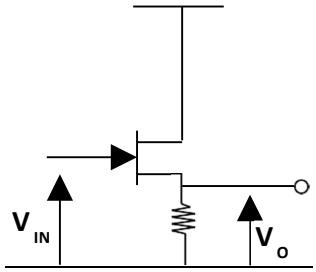
The configurations include:

Common Source



V
V O
IN

Common Drain (iii) Common Gate



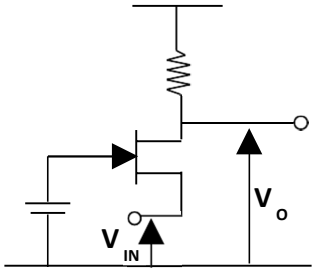
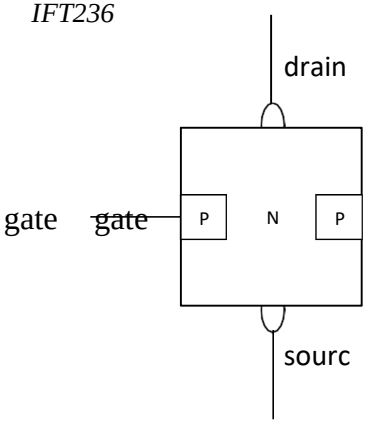


Fig 3.2 FET Configurations

The JFET is made up of a Semiconductor region known as the Channel with ohmic contacts at each end. The Channel material can either be N-type of P-type as shown below:



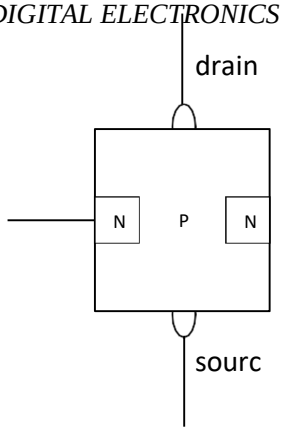


Fig 3.3 N channel JFET Fig 3.4 P channel JFET

The JFET is always operated with the Gate to Source voltage in Reverse Bias as shown below.

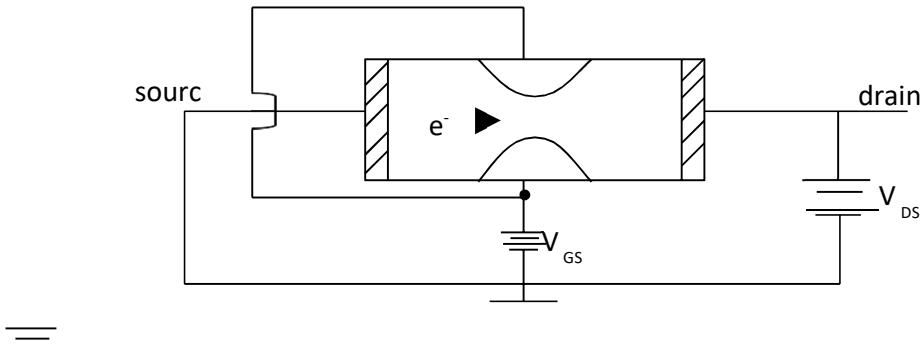


Fig 3.5 JFET Operation

In a P channel JFET, the P and N Junctions are reversed from those of the N Channel. In the P channel device, the Majority Carriers are holes (Positive Charges) and due to the low mobility of holes. The N-channel is often times preferred.

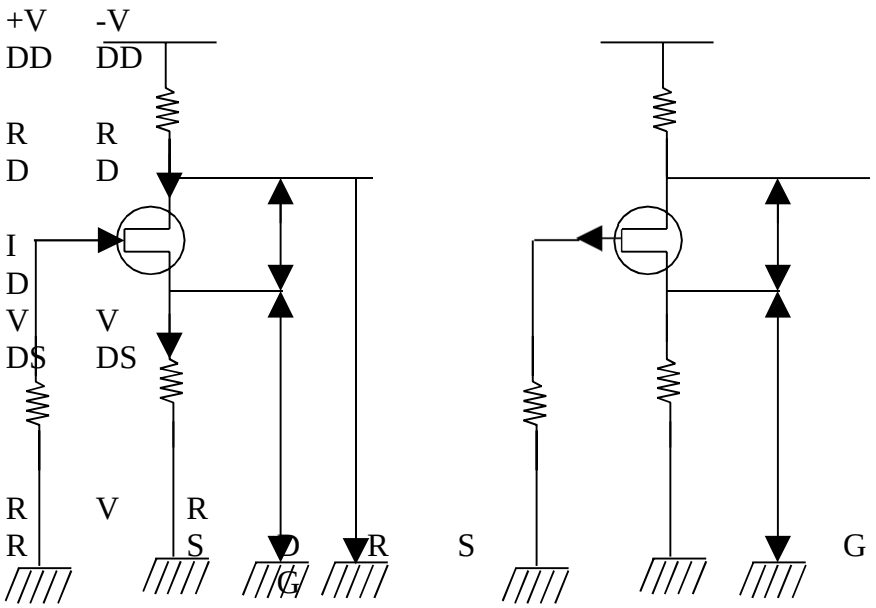
When VGS is increased, more positive ions are injected into the P side and this narrows the depletion region there by widening the channel and increasing the current flow. When VGS is decreased (made more negative), more positive ions are taken from the P side and the depletion region widens leading to a narrowing of the channel, reducing ID flow. When VGS becomes more negative to a point where ID=0, the conduction known as pinch-off arises.

Drain current at Pinch-Off is essentially zero. The PN JFET is a normally-On device and its current flow is controlled by the gate and can only be switched off by applying a suitable voltage to the gate terminal

For the JFET,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

Where IDSS = maximum value of ID when VGS = 0 VGS(off) = value of VGS when FET will be off



Example 1

Given IDSS = 12mA, VGS (off) = -5V, determine the value of ID at VGS = 0,
-1, -4.

Solution:

For $V_{GS} = 0$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2 = 12\text{mA}\left[1 - \frac{0}{-5V}\right]^2$$

$$=12\text{mA}\,[1 + 0]^2 = 12\text{mA}$$

For $V_{GS} = -1$

$$I_D = 12mA\left[1 - \frac{-1}{-5}\right]^2$$

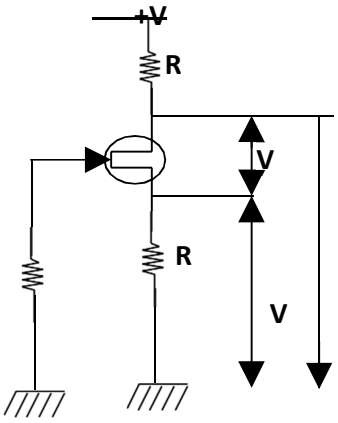
$$= 12mA\left[1 - \frac{1}{5}\right] = 7.68mA$$

For $V_{GS} = -4$

$$I_D = 12mA\left[1 - \frac{-4}{-5}\right]^2 = 12mA\left[1 - \frac{4}{5}\right]^2$$

$$= 0.48mA$$

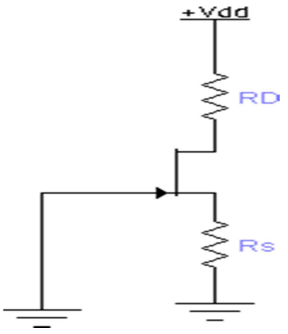
For the N channel JFET,



VDD □ IDRD □ VD
VD □ VDD □
VGS □ VG □
IDRD VS
R V VGS □
0 □ VS
VS □
IDRS
□ For N channel, the VGS = -IDRS For P channel, the VGS = IDRS
VDD □ IDRD □ VDS □ VS VS □ IDRS
VDD □
IDRD □ VDS □
IDRS
VDS □
VDD □
ID(RD □
RS)

Example 2

Given the circuit below with the following transistor parameters of IDSS = 5mA, Vp = VGS = -4V, design the circuit such that ID = 2mA, VDS = 6V



Solution

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{Vp}\right)^2$$

$$2 = 5\left(1 - \frac{V_{GS}}{-4}\right)^2$$

$$\left(1 - \frac{V_{GS}}{-4}\right) = \frac{2}{5}$$

Take the square root of both sides

$$\sqrt{\left(1 - \frac{V_{GS}}{-4}\right)^2} = \sqrt{0.4}$$

$$1 - \frac{V_{GS}}{-4} = 0.63$$

$$-\frac{V_{GS}}{-4} = 0.63 - 1 = -0.37$$

$$-V_{GS} = (-4)(-0.37) = 1.48$$

$$-V_{GS} = 1.48V$$

$$\therefore V_{GS} = -1.48V$$

From the diagram IDRS = -VGS
VGS
□ ID □ RS ——
□□ VGS
□ RS □ ID □

1.48 □ ——
2mA
0.74K□
From the output equation,

VDD □
IDRD □ VDS □
IDRS
VDS □
VDS □
VDD □
6V
ID □
IDRS
□ RD □
VDD □ VDS □ IDRS □
ID
10 □ 6 □ □ 2mA□ □ 0.74K□
2mA
RD □
4 □ 1.48 □
2
1.26K□

Example 3 Given the circuit below, the transistor parameters are IDSS = 12mA, Vp = -3.5V, R1+R2 = 100K. Design the circuit such that ID = 5mA, VDS = 5V

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)$$

$$5 = 12\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

$$\frac{5}{12} = \left(1 - \frac{V_{GS}}{-3.5}\right)$$

Square root both sides

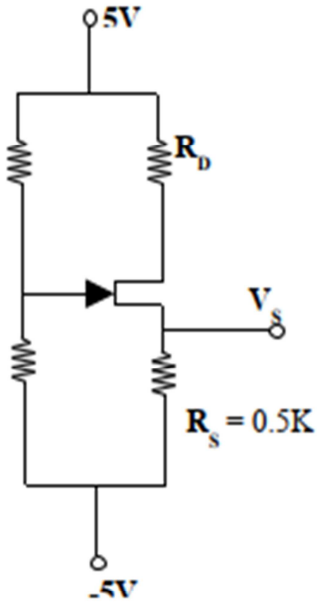
$$\sqrt{0.42} = \sqrt{\left(1 - \frac{V_{GS}}{-3.5}\right)}$$

$$0.65 = 1 - \frac{V_{GS}}{-3.52}$$

$$-\frac{V_{GS}}{-3.5} = -0.35$$

$$-V_{GS} = 1.24V$$

$$V_{GS} = -1.24V$$



From the circuit,

VS □
IDRS □ 5 □
□ 5□ □ 0.5□ □
5 □ □ 2.5V
VGS □
VG □ VS □ VG □
VGS □ VS
VGS □ □ 1.24 □ □ 2.5 □ □ 1.24 □ 2.5 □ □ 3.74V
From potential divider

VG □ R2 □ □ V □

R1 □ R2

□ 3.74 □ R2 □ 10□ □ 5
100
R2 □ 10□ □ □ 3.74 □ 5 100

R2 □
10
R2 □
R1 □
1.26K
12.6K
100K □
12.6K □
87.4K□
VDD □
IDRD □ VDS □
IDRS
□ RD □
VDD □ VDS □ IDRS □
ID
10 □ 5 □ □ 5□ □ 0.5□
5
RD □
10 □ 5 □
5
2.5 □
0.5K□

4.0 CONCLUSION

In this unit you have been introduced to the Field effect transistor amplifier and the different types of biasing arrangements and FET configurations.

5.0 SUMMARY

In this unit we have been able to extend knowledge of the theory and applications of transistors and transistor amplifier design.

6.0 TUTOR-MARKED ASSIGNMENT

Given IDSS = 12mA, VGS (off) = -4V, determine the value of ID at VGS = 0, -1, -4.

7.0 REFERENCES/FURTHER READING

Fitchen F.C; (1972). Transistor Circuit Analysis and Design. Second Edition Van Nostrand Reinhold Publishers.

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MODULE 2

Unit 1 Introduction to Feedback
Unit 2 Operational Amplifiers (OPAMPS)

UNIT 1 INTRODUCTION TO FEEDBACK

CONTENTS

1.0 INTRODUCTION

A feedback system is a system in which the input signal is modified by the system output before the internal processing by the system itself. The block diagram in a typical feedback system is shown in figure 4.1 below.

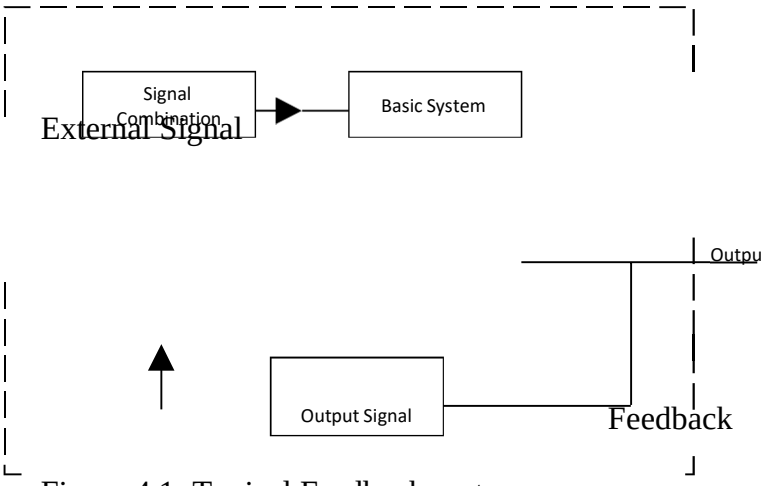


Figure 4.1: Typical Feedback system

The signal combination is usually a simple addition or subtraction. Multiplication, logical or other combination can also be used. The output signal processing is often a simple attenuation or amplitude reduction.

2.0 OBJECTIVES

At the end of this unit, students should be able to:

- be able to IDENTIFY feedback amplifier topologies
- be able to ANALYZE feedback amplifier topologies
- be able to DISCUSS the relative benefits and possible drawbacks of feedback amplifier topologies with respect to basic amplifier topologies
- be able to APPLY the concepts of feedback analysis to the DESIGN of analog amplifiers to meet or exceed stated specifications.

3.0 MAIN CONTENT

Feedback Amplifiers

A feedback amplifier consists of two parts

The Amplifier system
The feedback system

The classic block diagram for a feedback system is given in figure 4.2 below.

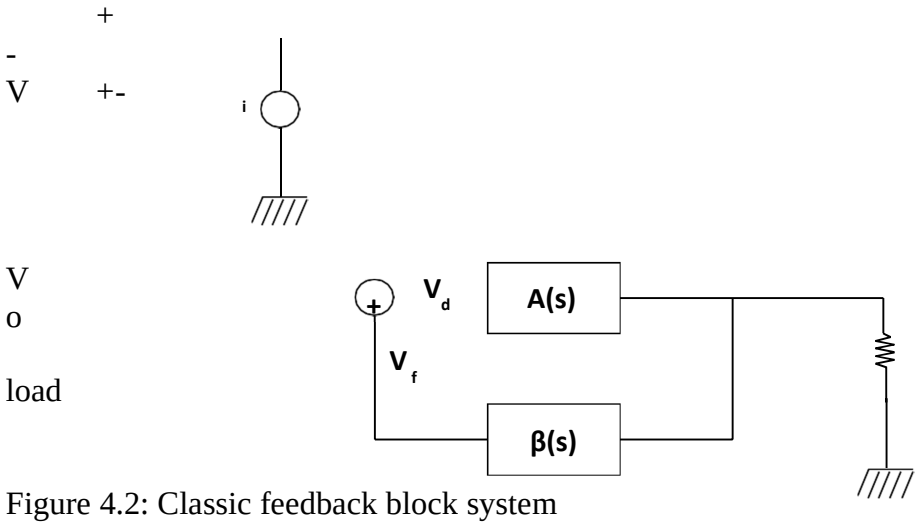


Figure 4.2: Classic feedback block system

The amplifier A(s) when used without the feedback is said to be in open loop with the gain denoted by A01.

From the circuit in figure 4.2 above.

Vd □ Vi □ Vf Vo □ A01Vd
(1)
(2)
Vf □ □ Vo
(3)

From equation (2), substitute for Vd

Vo □
A01□Vi □ Vf □
But Vf
□ □ Vo

$$Vo = A01(Vi - \beta Vo) \quad (4)$$

Expand (4) and collect like terms

$$Vo = A01Vi - A01\beta Vo$$

$$A01Vi = Vo + A01\beta Vo = Vo(1 + A\beta) \quad (5)$$

$$A01Vi = Vo(1 + A01\beta)$$

$$\therefore \frac{Vo}{Vi} = \frac{A01}{1 + A01\beta} = ACL \quad (6)$$

The Voltage
The Voltage gain for the closed loop is given to be
ACL □
Vo □
Vi
A01

1 □ A01□

A01 = open loop gain

β = feedback attenuation factor A01β = loop gain = T
ACL □
A01

1 □ T

Types of Feedback Arrangements

There are two basic types of feedback arrangements and these are:

Positive Feedback

In the positive feedback arrangement, the feedback voltage is in the same phase as the input voltage and it increases the input voltage amplitude. It leads to instability in systems and is only used in oscillator design.

For Positive Feedback (PFB)

Vd □ Vi □ Vf
Vo □
A01Vd
Vo □
A01□Vi □ Vf □ □
A01□Vi □ □ Vo□
Vo □
A01Vi □
A01□ Vo
A01Vi □
Vo □A01□ Vo □
Vo□1 □
A□ □
Vo □ 1 □ A01

Vi A01□
□ ACL □
Vo □
Vi
A01
1 □ A01□
PFB
Negative Feedback

In negative feedback, the feedback voltage is 1800 out of phase with the input voltage. This leads to a reduction in the input voltage and this stabilizes the system. It is used mostly in amplifier.

Negative Feedback (NFB)

$$Vd = Vi - Vf$$

$$Vo = A_{01}Vd$$

$$Vo = A_{01}(Vi - \beta Vo) = A_{01}Vi - A_{01}\beta Vo$$

$$A_{01}Vi = Vo + A_{01}\beta Vo = Vo(1 + A_{01}\beta)$$

$$\frac{Vi}{Vo} = \frac{1 + A_{01}\beta}{A_{01}}$$

$$\therefore A_{CL} = \frac{Vo}{Vi} = \frac{A_{01}}{1 + A_{01}\beta} \quad \text{——————} \quad \text{NFB}$$

Both gain A and feedback β may be complex quantities having both a modulus and an angle which may depend on signal frequency.

A01□ □
ACL □————————
1 □ □ A01□ □□
□ □ □

For NFB, T = Positive > 0 For PFB, T = Negative < 0

SELF ASSESSMENT EXERCISE

The gain and feedback factor of an amplifier at different frequencies are listed below. For each case, determine the nature of the feedback and system gain.

F1	F2	F3	F4
A 5000<180°	4500<160°	1000<65°	500<20°
β 0.02<0°	0.018<-5°	1.148 x 10-3<-10°	0,001<-15°

F1 ACL
□ 500 □ 180 □
1 □ 100 □ 180
5000 □ 180 □
101 □ 180

49.5 □ 1800
Solve the rest.

From our previous discussion, the gain of an amplifier (Voltage gain) without feedback is higher than the gain with negative feedback while it is lower than the gain of the amplifier with positive feedback.
AV(NFB) < AV < AV(PFB).

Effect of Negative Feedback on Amplifiers

Gain and Gain Stability

Typical amplifiers are subject to changes such as temperature, dc supply levels and ageing. Such change results in variation in amplifier gain. Negative feedback helps to reduce the variation in gain to acceptable limits (or stabilize the gain).

For a NFB amplifier

ACL □
A01

1 □ A01□
A01β>>1
ACL □
A01 □ 1

A01□ □

The feed back ration β is often determined by the ratio of two resistors.

Example 1
The gain of an amplifier is found to be 750 on test but under conditions of reduced dc supply and external loading, the value reduced to 400. Compare this percentage variation for the amplifier with the corresponding variation if NFB of (a) 0.005 (b) 0.03 (c) 0.1 is used.

Solution
Percentage variation of gain without feed back is original □ new □ 100 □ 750 □ 400 □ 100 □

46.67 %
original 1 750 1
Using a β of 0.005

$$\text{The maximum gain} = \frac{A}{1 + A\beta} = \frac{750}{1 + (750 \times 0.005)} = \frac{750}{4.75} = 157.9$$

$$A\min = \frac{400}{1 + (400 \times 0.005)} = 133.3$$

$$percentage\ variation = \frac{157.9 - 133.3}{157.9} \times \frac{100}{1} = 15.6\%$$

From this we observe that the gain of the amplifier now ranges from 157.9 to 133.3 as against the 750 to 400 and the variation is now 15.6% as against 46.7%.

Using a β of 0.03
A max □
A min □
1 □ □
1 □ □
750
750 □

400
400 □
0.03□ □
0.03□ □
31.9
30.8
31.9 □ 30.8
100
percentage variation □
31.9
□ 1 □
3.45 %

From the above, as the β increases, the gain reduces and the stability increases. Thus, negative feedback decreases gain but increases stability.

Decreased Distortion
Amplifiers exhibit a measure of non-linearity due to the curvature of the characteristic curve of active (cut off and saturation points). The non-linearity results in harmonic distortion and Clipping. Each output without distortion has a harmonic distortion component D.

Vout □
AVin □ D
(1)

From the feed back definition (PFB)

$$Vin = Vi + \beta Vo \quad \text{——————————} \quad (2)$$

But $Vo = AVin + D$ ——————————— (3)

$\therefore Vin = Vi + \beta AVin + \beta D$ Expanding

$Vin = Vi + \beta AVin + \beta D$ Collecting like terms

$Vin - \beta AVin = Vi + \beta D$

$Vin(1 - \beta A) = Vi + \beta D$

$$Vin = \frac{Vi + \beta D}{1 - \beta A}$$ Substitute in equation 3

$$Vo = A\left(\frac{Vi + \beta D}{1 - \beta A}\right) + D$$ Taking LCM

$$\frac{AVi + A\beta D}{1 - \beta A} + D$$

$$\frac{AVi + A\beta D + D(1 - \beta A)}{1 - \beta A} = \frac{AVi + A\beta D + D - A\beta D}{1 - \beta A}$$

$$Vo = \frac{AVi + D}{1 - \beta A} = \frac{AVi}{1 - \beta A} + \frac{D}{1 - \beta A}$$

AVi
The term 1 □ □ A
= actual amplified signal.
D

1 □ □ A
= Distortion

The distortion present in the signal is reduced by a factor of (1- βA) while the desired output can be attained by controlling Vi.

When negative feedback is used, the distortion level will be reduced by a factor (1 + βA).

Example 2

In an amplifier without feedback, the gain is 36dB and the harmonic distortion at normal output level is 10%. Determine.

The gain
The distortion

When NFB is applied with the feedback factor of 16dB, Feedback factor = loop gain = βA

Solution

$$Acl = \frac{A}{1 + \beta A} \qquad \text{Gain (dB)} = 20\log A$$

For no feed back

$36 = 20\log A \qquad \therefore A = 10^{1.8} = 63$

Feed back factor = $16 = 20\log\beta A$

$\beta A = 10^{0.8} = 6.3$

$\beta A = 6.3$ but $A = 63$

$$\therefore \beta = \frac{6.3}{63} = 0.1$$

Gain using NFB

Gain using NFB

$B = 0.1$

$$Acl = \frac{63}{1 + 63 \times 0.1} = \frac{63}{7.3} = 8.63$$

$20\log 8.63 = 18.7\text{dB}$

$$\text{Distortion} = \frac{D}{1 - \beta A} = \frac{0.1}{7.3} \times 100 = 1.36\%$$

Increased Bandwidth

Amplifiers have a frequency range over which the gain and phase shift are approximately constant. For frequencies outside the band (mid-band range), the gain falls. When NFB is applied, the gain drops. The product of the gain and bandwidth must remain constant; so as the gain drops by a factor, the bandwidth increases by that same factor.

Example 3

An RC coupled amplifier has a frequency gain of 300 and a response from 100Hz to 20KHz. A negative feedback with β = 0.02 is incorporated into the circuit. Determine the new system performance.

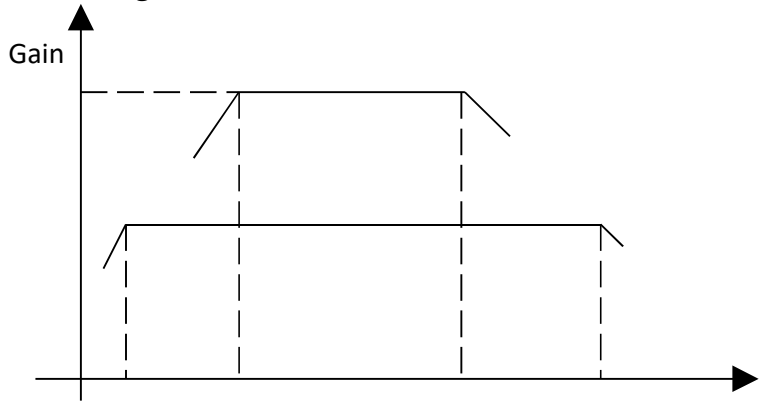
Solution

$$A' = \frac{A}{1 + A\beta} = \frac{300}{1 + 300 \times 0.02} = 42.85$$

$$f1' = \frac{f1}{1 + A\beta} = \frac{100}{1 + 300 \times 0.02} = 14.28Hz$$

$$f2' = f2(1 + A\beta) = 20KHz(7) = 140KHz$$

From the diagram



F ′ 1
14.28
F
1
100

F
2
20K

F ′ 2
140K
Frequency

From the values above, applying the gain product bandwidth equation,
A (Bandwidth) = A′ (Bandwidth′)
A (f2 – f1) = A′ (f2 – f1′)

300 (20 KHz – 100Hz) = 42.85 (140 KHz – 14.28Hz)

5.97MHz = 5.99MHz

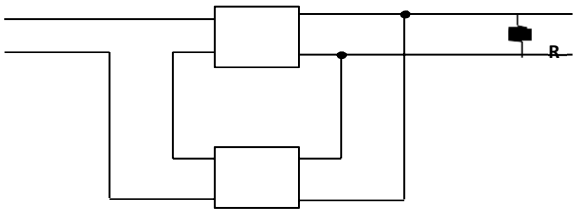
From the values above

A (f2 – f1) ≈ A′ (f2′ – f1′)

3.4 Types of Negative Feedback Circuit Topologies

There are basically 4 types of feedback amplifier circuit topologies depending on how the signals are added at the input.

Shunt Derived Series-Fed Feedback



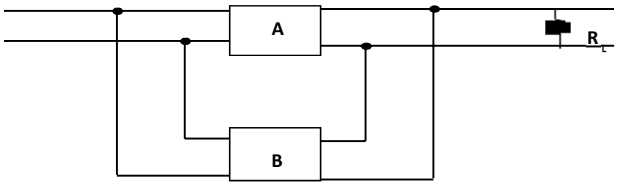
This is also known as Voltage Series Feedback. The output is connected in parallel while the input is connected in series.

The output resistance is reduced by the shunting effect of the feedback connection while the input resistance is increased by the series addition of both the feedback and amplifier resistance values.

$$Ro' = \frac{Ro}{1 + \beta A}$$

$$Ri' = Ri(1 + \beta A)$$

Shunt Derived Shunt-Fed Feedback Topology

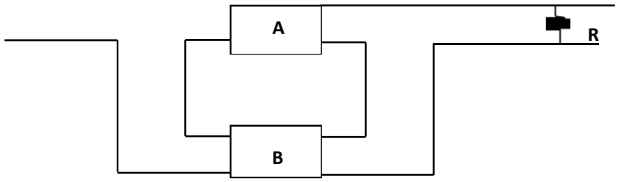


In this arrangement, the feedback is connected to both the input and output of the amplifier in parallel. This leads to a reduction in both the input and output impedance values.

$$Ro' = \frac{Ro}{1 + \beta A}$$

$$Ri' = \frac{Ri}{1 + \beta A}$$

Series Derived Series-Fed Feedback Topology

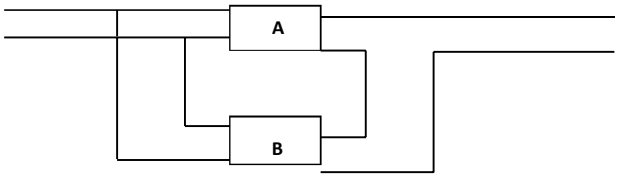


In this arrangement, the input and output of the amplifier are connected in series. This leads to an increase in both input and output impedance.

$$Ro' = Ro(1 + A\beta)$$

$$Ri' = Ri(1 + A\beta)$$

Series Derived Shunt-Fed Feedback Topology



In this arrangement, the output is feedback in series and the input is connected in parallel. The output impedance is increased by the factor 1+A β while the input impedance is decreased.

$$Ro' = Ro(1 + A\beta)$$

$$Ri' = \frac{Ri}{1 + A\beta}$$

The application of negative feedback has the following summarized effects.

Decreases the effect of noise
Decreases the voltage gain
Decreases the Harmonic distortion
Increases Gain stability
Increases System bandwidth

Its effect on the input and output impedance values depends on the topology used.

4.0 CONCLUSION

The advantages and applications of feed back has been studied in this unit and the different applications and advantages of the negative feedback for amplifier design has also been studied.

5.0 SUMMARY

In this unit we studied the following:

The application of negative feed back
The effects of negative feed back.
The determination of the gain of a positive and negative feed back amplifier system.

6.0 TUTOR-MARKED ASSIGNMENT

Determine the input resistance of a shunt input connection and the output resistance of a series output connection for a feedback amplifier. Open loop gain = 105. Closed loop gain =50.Input and Output resistance of the basic amplifier are 10kΩ and 20kΩ respectively.

Calculate the percentage change in the closed loop gain and a change in the open loop gain. Open loop gain = 105. Closed loop gain =50,β = 0.01999.Assume a change in the open loop gain is 104

Given a negative feedback circuit with the following parameters Open loop gain = 106. Closed loop gain = 100. If the magnitude of the open

loop gain decreases by 20% determine the corresponding change in the closed loop gain.

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Neamen D.A (1996). Electronics Circuit Analysis and Design.

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UNIT 2 OPERATIONAL AMPLIFIERS (OPAMPS)

CONTENTS

1.0 INTRODUCTION

The operational amplifier is a direct coupled amplifier capable of amplifying signals from DC up to a few MHz An operational amplifier—or op-amp—can perform a great number of operations, such as addition, filtering, or integration, which are all based on the properties of ideal amplifiers and of ideal circuit elements. The introduction of the operational amplifier in integrated circuit form marked the beginning of a new era in modern electronics. Since the introduction of the first IC op-amp, the trend in electronic instrumentation has been to move away from the discrete (individual-component) design of electronic circuits, toward the use of integrated circuits for a large number of applications. The majority of op-amps have three stages. The first stage converts the differential signal into a single-ended one; the second one provides the bulk on the gain and the third one the required output power.

2.0 OBJECTIVES

At the end of this unit, student should be able to:

- be able to IDENTIFY op-amp circuit topologies
- be able to ANALYZE op-amp circuits
- be able to DISCUSS the relative properties of op-amp circuits.

3.0 MAIN CONTENT

Ideal Op-Amp

The Ideal Op Amp parameters are derived to simplify circuit analysis. Op amps depart from the ideal in two ways. First, dc parameters such as input offset voltage are large enough to cause departure from the ideal.

The ideal assumes that input offset voltage is zero. Second, ac parameters such as gain are a function of frequency, so they go from large values at dc to small values at high frequencies. The table below lists the ideal opamp parameters.

Table 5.1 Ideal Opamp assumptions

PARAMETER NAME	PARAMETERS SYMBOL	VALUE
Input current	I_{IN}	0
Input offset voltage	V_{OS}	0
Input impedance	Z_{IN}	∞
Output impedance	Z_{OUT}	0
Gain	a	∞

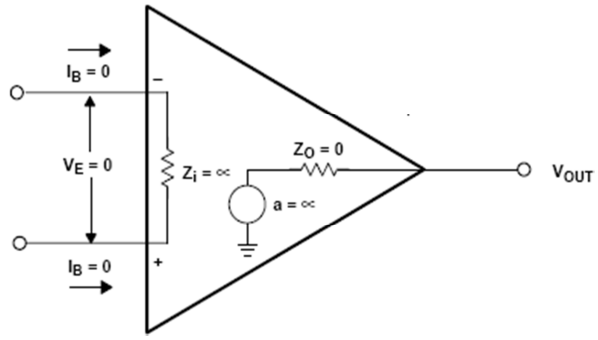


Figure 5.1 ideal Opamp

Op-Amp Configurations

There are two basic configurations of the operational amplifier and these are:

The Noninverting Op Amp

The noninverting op amp configuration has the input signal connected to its noninverting input. There is no input offset voltage because VOS = VE = 0, hence the negative input must be at the same voltage as the positive input. The op amp output drives current into RF until the negative input is at the voltage, VIN. This action causes VIN to appear across RG. The voltage divider rule is used to calculate VIN; VOUT is the input to the voltage divider and VIN is the output of the voltage divider. Since no current can flow into either op amp lead.

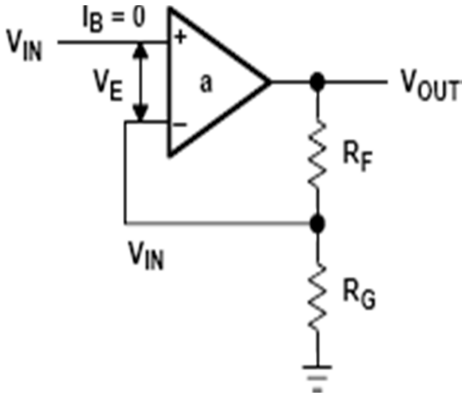


Figure 5.2 Non inverting opamp configurations

From the circuit shown in the fig above, the gain of the noninverting configuration is derived as:

$$V_{IN} = V_{OUT}\frac{R_G}{R_G + R_F}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_G + R_F}{R_G} = 1 + \frac{R_F}{R_G}$$

The Inverting Op Amp

In the inverting configuration, the input is fed through the input resistor to the inverting pin and the noninverting input of the inverting op amp circuit is grounded. One assumption made is that since the opamp has an infinite input resistance, so the feedback keeps inverting the input of the opamp at a virtual ground (not actual ground but acting like ground). The current flow in the input leads is assumed to be zero, hence the current flowing through RG equals the current flowing through RF. Using Kirchoff's law, and the Equation is written with a minus sign inserted because this is the inverting input. Algebraic manipulation gives.

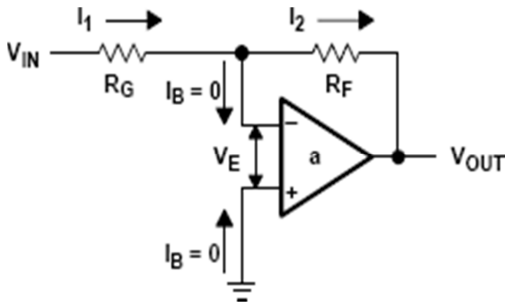


Figure 5.3 Inverting opamp configurations

From the inverting Opamp configuration the gain is derived is follows:

I1 □
VIN RG
□ □ I 2 □
VOUT
RF
VOUT VIN
□ □ RF
RG

Notice that the gain is only a function of the feedback and gain resistors, so the feedback has accomplished its function of making the gain independent of the op amp parameters. The actual resistor values are determined by the impedance levels that the designer wants to establish. If RF = 10 k and RG = 10 k the gain is minus one as shown in Equation.

Applications of Op-Amps

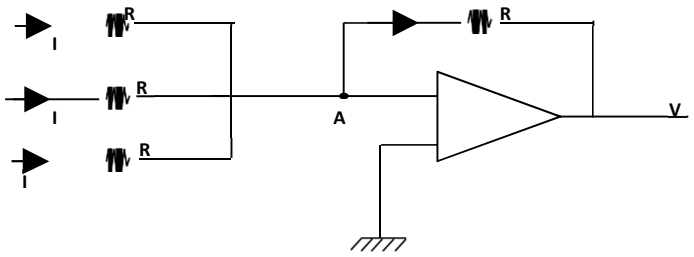
The operational amplifier can be configured to perform mathematical operations. Some of these are listed below:

Adder or Summer

The adder circuit of the operational amplifier provides an output voltage proportional to the algebraic sum of the inputs, each multiplied by a constant gain factor.

V

V V



I1 □
V 1 , I 2 □
R1
V 2 , I 3 □
R2
V 3 , IF □ VF
R3 RF

From Kirchoff's current law at point A I1 + I2 + I3 = IF

V 1 □
R1

V 2 □
R2

V 3 □ □ Vo R3 RF

Multiply through by RF

$$\frac{V_1}{R_1}R_F + \frac{V_2}{R_2}R_F + \frac{V_3}{R_3}R_F = -V_o$$

$$\frac{R_F}{R_i} = A_V$$

$$\therefore V_1A_{V1} + V_2A_{V2} + V_3A_{V3} = -V_o$$

Assuming $R_1 = R_2 = R_3$

$$-V_o = \frac{V_1R_F}{R} + \frac{V_2R_F}{R} + \frac{V_3R_F}{R}$$

$$V_o = -\frac{R_F}{R}(V_1 + V_2 + V_3) = A_V(V_1 + V_2 + V_3)$$

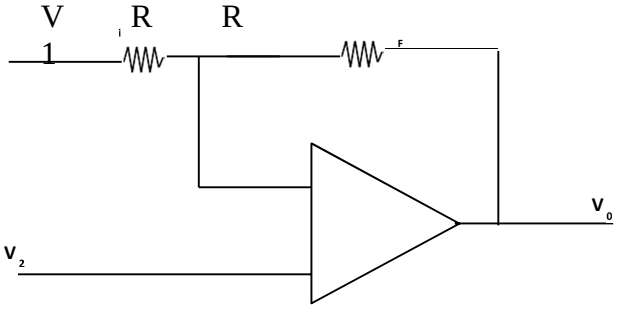
If $R_F = R$

$$V_o = -(V_1 + V_2 + V_3)$$

Hence the output is proportional to the sum of the output voltages.

Subtractor

The function of the subtractor is to produce an output proportional to the difference of the two input signals.



Using superposition theorem, the sum of the output with the input taken one by one is as listed below.

V01 = output generated by V1 V02 = output generated by V2

$$V_{01} = -\frac{R_F}{R_i}V_1$$ ——————— Inverting amplifier

$$V_{02} = \left(1 + \frac{R_F}{R_i}\right)V_2$$ ——————— Non-inverting amplifier

$$R_F >> R_i, \qquad \frac{R_F}{R_i} >> 1$$ (Rule of Thumb)

$$V_o = -\frac{R_F}{R_i}V_1 + \frac{R_F}{R_i}V_2$$

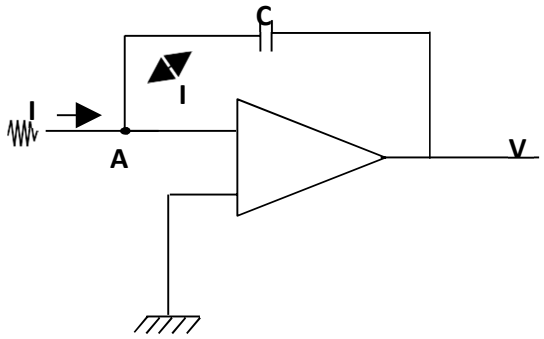
$$V_o = \frac{R_F}{R_i}(V_2 - V_1)$$

$$V_o = A_V(V_2 - V_1)$$

Integrator

Integration is a mathematical process of determining the area under a curve. The Op amp integrator produces an output that is proportional to the area under the curve of the input voltage.

V R



From the concept of virtual ground, Point A = 0

$Vin = IR \qquad \therefore I1 = \frac{V1}{R}$

The current through the capacitor charges it in the direction shown below.

$I2 = -\frac{Vout}{Xc} \qquad \therefore I1 - I2 = 0$

$Xc = \frac{1}{2\pi fC} = \frac{1}{jwC} = \frac{1}{sC}$

$jw = s$

$jw = s$

$\frac{Vi}{R} = -\frac{Vout}{1/sC} = VoutsC$

$\therefore Vout = -\frac{Vi}{sRC}$

Voltage gain $= \frac{Vo}{Vi} = -\frac{1}{sRC}$

Converting this to time domain

$Vo = -\frac{1}{RC}\int_0^t Vi(t)dt$

Alternatively

$I_1 = I_2$ where I_2 = Current through the capacitor

$I2 = C\frac{dVc}{dt}$ but $Vc = Vo$

$\frac{dVc}{dt} = \frac{I2}{C}$ but $I1 = I2 = -\frac{Vi}{R}$

$\frac{dVout}{dt} = -\frac{V1}{RC} \qquad \therefore dVout = -\frac{V1}{RC}dt$

Integrating both sides

$$Vout = -\frac{1}{RC}\int_0^t Vidt$$

The integrator is a low pass filter and produces more output for low frequency signals.

Example 1

A 5V, 1KHz sinusoidal signal is applied to the input of an op amp integrator. R = 100K, C = 1μF, determine the Vout.

Vin = 5 Sin 2πft = 5 Sin 2000πt. Integration is from t = 0 to t = t

$$Vo(t) = -\frac{1}{RC}\int Vin(t)$$

$$-\frac{1}{RC} = -\frac{1}{100 \times 10^3 \times 1 \times 10^{-6}} = -10$$

$$Vo = -10\int_0^t 5Sin200\pi t = -50\left[-\frac{Cos2000\pi t}{2000\pi}\right]_0^t$$

$$= \frac{1}{40\pi}(Cos2000\pi - 1)$$

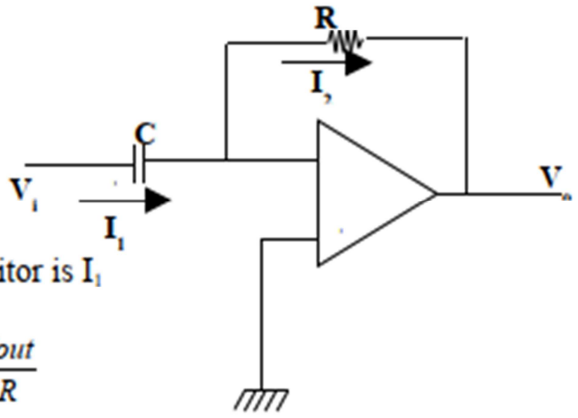
Differentiator

This is the process by which the rate of change of a curve at any given point can be determined. It is essentially the inverse of integration.

$$Vin = I_1 Xc \qquad \therefore I_1 = \frac{Vin}{Xc}$$

$$I_2 = -\frac{Vout}{Xc} \qquad I_1 = I_2$$

$$\frac{Vin}{X} = -Vout$$



But the current through the capacitor is I_1

$$\therefore I_1 = C\frac{dVin}{dt} \qquad \therefore C\frac{dVin}{dt} = -\frac{Vout}{R}$$

$$Vout = -RC\frac{dVin}{dt}$$

The differentiator is basically a high pass filter.

4.0 CONCLUSION

In this unit you have been introduced to the operational amplifier and its applications.

5.0 SUMMARY

In this unit we have been able to extend knowledge of the theory and applications of operational amplifiers and the basic configurations of op amps.

6.0 TUTOR-MARKED ASSIGNMENT

A 5V, 10 KHz sinusoidal signal is applied to the input of an op amp integrator for 10 seconds. R = 100K, C = 1μF, determine the Vout.

7.0 REFERENCES/FURTHER READING

Fitchen F.C; (1972). Transistor Circuit Analysis and Design. Second Edition Van Nostrand Reinhold Publishers.

Maddock R.J and Calcutt D.M (1994). Electronics: a Course for Engineers Second Edition. Longman Publishers.

Neamen D.A (1996). Electronics Circuit Analysis and Design.

McGraw-Hill Publishers.

MODULE 3 BOOLEAN ALGEBRA, LOGIC GATES, AND COMBINATIONAL CIRCUITS

MODULE INTRODUCTION

This module is designed to enables the student get a good understanding of one of the critical foundations of digital electronics. It covers the mathematics of Boolean algebra which leads to logic minimizations, and then moves to logic gates and combinational circuits.

Unit 1 Boolean algebra
Unit 2 Logic gates – Types, circuits symbols, and truth tables
Unit 3 Karnaugh maps and logic circuit minimizations
Unit 4 Combinational circuits – Arithmetic & Logic functions: Adders, Subtractors, Comparators
Unit 5 Combinational circuits – Data transmission : Multiplexers, Demultiplexers, Encoders, Decoders
Unit 6 Combinational circuits – Code converters: Binary, BCD, 7-segment

UNIT 1 BOOLEAN ALGEBRA

CONTENTS

1.0 INTRODUCTION

The objective of this course is to introduce the student to the field of digital systems. Starting at the fundamental level of Boolean algebra and the different laws used in the resolution of digital electronics circuits.

2.0 OBJECTIVES

At the end of this unit, students should be able to:

- the understanding of Boolean algebra and its laws
- the introduction of the Boolean algebraic identities
- the introduction of the De Morgan’s theorem.

3.0 MAIN CONTENT

Boolean Algebra

Boolean algebra is the basic mathematics for the study of logic design .Basic laws of Boolean algebra are implemented as switching devices called logic gates. A Boolean variable can take on two values ‘0’ and ‘1’, ‘T’, ‘F or H,L or ON,OFF . Boolean operations transform Boolean Variables the basic operations are NOT, AND, OR.

More complicated Boolean Functions can be derived from the basic Boolean operations.

Basic Boolean algebraic identities

A + 0 = A A + 1 = 1 A + A = A A + A = 1 0*A = 0
1*A = A A*A = A A*A = 0
A □ A

=
Laws of Boolean algebra Commutative Law
A + B = B + A
A B = B A

Associate Law

(a) (A + B) + C = A + (B + C)
(b) (A B) C = A (B C)

Distributive Law

(a) A (B + C) = A B + A C
(b) A + (B C) = (A + B) (A + C)

Identity Law

A + A = A
A A = A

Redundance Law

A + A B = A
A (A + B) = A

Other Boolean Identities

(a) $A\bar{B} + AB = A$

(b) $(A+B)(A+\overline{B}) = A$

$\overline{A} + A = 1$

$\overline{A}\ A = 0$

$A + \overline{A}\ B = A + B$

$A\ (\overline{A} + B) = A\ B$

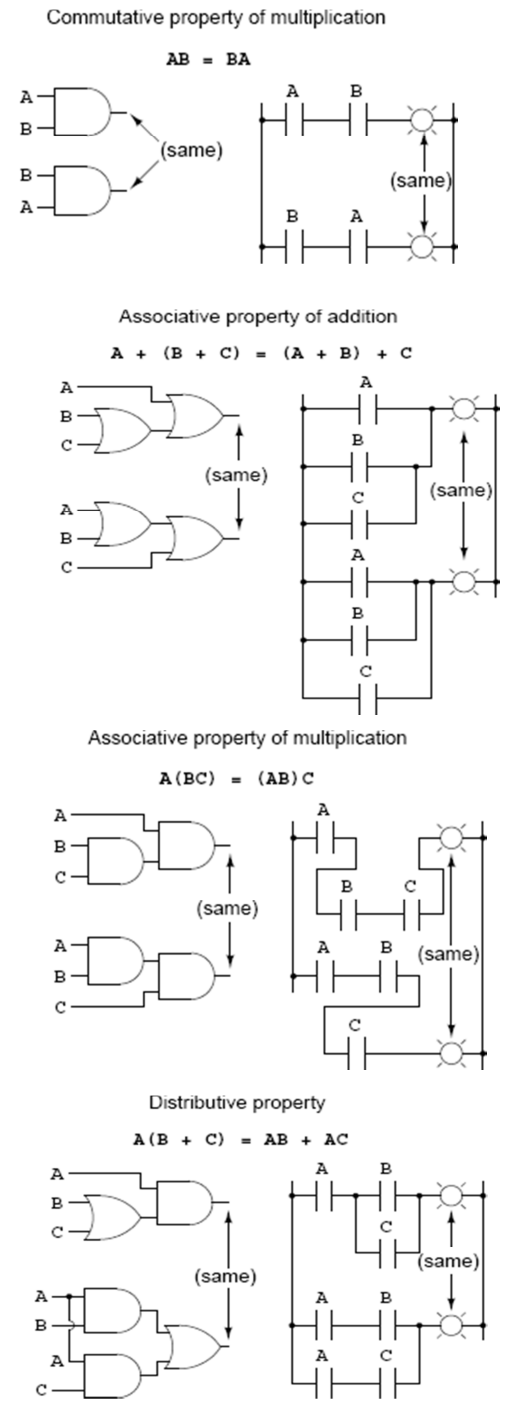


Fig 9.1 Boolean algebraic identities

Example 1 Prove (a) A □

Solution

$\overline{A}B$ □ A □ B

Algebraically:

A □ AB □ $\overline{A}$1 □ $A\overline{B}$

□ A(1 □ B) □ AB
□ A □
□ A □
□ A □□□

AB □ AB B(A □ A) B
Using the truth table:

Table 9.1: Truth table for the example 9.1

A	B	A+B	$\overline{A}B$	$\overline{A}$+ AB
0	0	0	0	0
0	1	1	1	1
1	0	1	0	1
1	1	1	0	1

DeMorgan's Theorem

DeMorgan's Theorem allows gates to be converted to others by simply inverting the inputs of the selected gate. More specifically, you can convert gates to others if the following steps are followed accordingly:

Complement all inputs.
Convert all AND operations to ORs
Convert all OR operations to ANDs
Complement the entire expression.

A □ B □ $\overline{A \square \overline{B}}$

$\overline{A \square B}$ □ $\overline{A}$ □ $\overline{B}$

The key to the theorem is break the line, change the sign

The truth table to prove the theorem is shown below.

A	B	$\overline{A}$	$\overline{B}$	$\overline{A \cdot B}$	$\overline{A} \cdot \overline{B}$	$\overline{A + B}$	$\overline{A} + \overline{B}$
0	0	1	1	1	1	1	1
0	1	1	0	0	0	1	1
1	0	0	1	0	0	1	1
1	1	0	0	0	0	0	0

4.0 CONCLUSION

In this unit you have been introduced to the basic principles of the Boolean algebra and the demorgans theorem.

5.0 SUMMARY

In this unit we have been able to extend knowledge of the theory and applications of Boolean algebra, the De Morgan's theorem and the different rule that govern the use of Boolean algebra in digital electronics.

6.0 TUTOR-MARKED ASSIGNMENT

Simplify the expression using Boolean algebra

$x y \cdot \overline{x}\,\overline{y} \cdot \overline{xy}$

$\overline{x} \cdot xy \cdot$

$\overline{x}z \cdot$

$\overline{x}\,\overline{y}\,z$

$[\overline{AB} \cdot (C \cdot BD) \cdot$

$\overline{A}\,\overline{B}] C$

$\overline{A}BC \cdot$

$\overline{AB}\,C \cdot$

$\overline{A}\,\overline{B}\,C \cdot$

$\overline{AB}\,C \cdot$

ABC

Apply DeMorgan's theorems to the following expression

$\overline{A \cdot BC} \cdot \overline{D(E +)}$.

7.0 REFERENCES/FURTHER READING

Fitchen F.C; (1972). Transistor Circuit Analysis and Design. Second Edition Van Nostrand Reinhold Publishers.

Maddock R.J and Calcutt D.M (1994). Electronics: a Course for Engineers Second Edition. Longman Publishers.

Neamen D.A (1996). Electronics Circuit Analysis and Design.
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UNIT 2 LOGIC GATES – TYPES, CIRCUIT SYMBOLS, AND TRUTH TABLES

CONTENTS

1.0 INTRODUCTION

A logic gate is an electronic circuit which makes logic decisions. It has one output and one or more inputs. They are the fundamental blocks with which digital systems are built. The output is a result of the implementation of the logical algebra known as the Boolean algebra.

2.0 OBJECTIVES

At the end of this unit, student should be able to:

identify the different logic gates
analyze circuits with logic gates
generate other gates from the universal gates.

3.0 MAIN CONTENT

3.1 Logic Gates

One characteristic of this Boolean algebra is that the variables can only assume one of the two values 0 and 1. Where 0 (zero) can represent off, low, minus or false depending on the convention used while 1 (one) takes the opposite state. The gates are available in various IC families, popular among them are the transistor- transistor logic (TTL), emitter

coupled logic (ECL), metal oxide semiconductor (MOS) and the complementary metal oxide semiconductor (CMOS). Most of these families have their unique characteristics and qualities for example, the TTL families consume considerable quiescent current while the CMOS which is factor than the TTL consumes zero quiescent current (though it is more delicate) among other properties.

We shall be considering the following gates and their truth table OR gate, AND gate, NOT gate, NOR and NAND gates. Another gate we will look at is the exclusive OR gate. The logic used to determine the state of the variables can either be positive or negative. In the positive logic, where there are two voltage values, the more positive of the voltage represents the high while if we are operating on the negative logic, the more negative value would represent the high state.

3.2 OR Gate

The OR gate is a gate which produces a high output of any or both (all) if its inputs are high. It symbolizes logic addition.

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

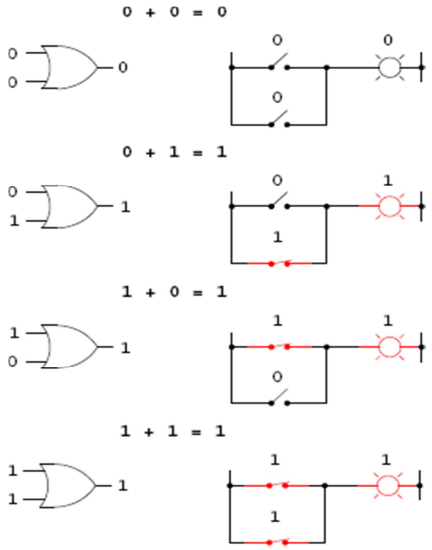


Figure 2 input OR gate

From the diagram (b) we see that so long as any of the switches is closed the bulb will light up. The OR gate represents the Boolean equation;

$$A + B = C$$

NOTE: a truth table is a table which gives the output state for all the possible input combination.

This OR gate can also be known as an inclusive OR gate because it includes the case when both input are true. Gates can have any number of inputs but standard packages contain four 2- input gates, three 3-input gates. The OR gate can also be derived from discrete circuits. e.g. diodes and transistors.

3.3 AND Gate

The AND gate is a logic gate which will give a high output if and only if all its inputs are high. It symbolizes logical multiplication.

SYMBOL

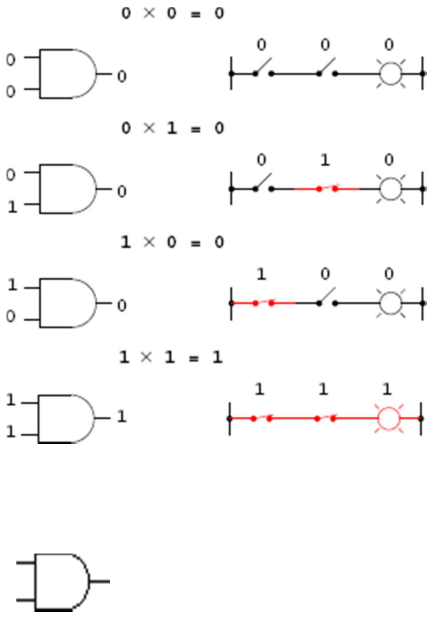


Figure 2 –input AND gate

The AND gate works on the Boolean algebra

$$A \times B = C$$

From the diagram it can be seen that an AND gate can be represented by a series circuit. For the lamp to come on, the switches A and B must be on. Below are truth tables for two and three input AND gates.

Two input AND gate. C = output Three input AND gate. D = output

The AND gate can also be realized using the diode and the transistor.

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0

3.4 The NOT Gate (Inverse)

The NOT gate is also known as an inverter because it inverts the input signal. It has one input and one output terminal. The logical symbol for negation or inversion is a bar over whose function is to indicate the opposite state. The symbol of the NOT gate is shown below. Truth table for the NOT gate

A	B
0	1
1	0

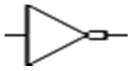


Figure 3 NOT gate symbol

$B = \overline{A}$

3.5 The NOR Gate

The NOR gate is a combination of the NOT and the OR gate. The NOT gate function is a reverse of the OR gate function so it will have an output of 1 only when all its inputs are 0. The output of the NOR gate is fed to the input of the NOT gate to give NOR.

The NOR gate is also referred to as a universal gate because it can be used to simulate OR, AND and NOT gate functions. The NOR gate symbol is an OR gate symbol with a bubble at the output pin as shown below.

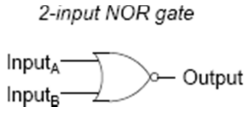
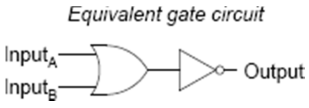


Figure 4-input NOR gate



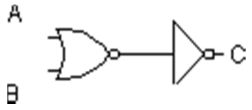
Truth table for the 2 input NOR gate

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

OR GATE FUNCTION

By placing another inverter at the output of the NOR gate the output is inverted giving an OR gate function.

OPERATION

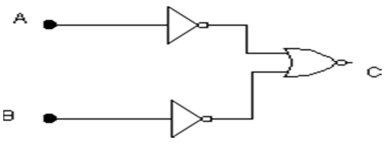


A + B = $\overline{\quad}$

A □ B = C

AND GATE FUNCTION

In this case, two inverters are used in the input. The inputs are inverted before going into the NOR gate and thus the output of the NOR gate is:



$$C = A + B$$

NOT GATE FUNCTION

In this case the two inputs are tired together and the output is A + A which by demorgan is A. the OR and AND gates can also be derived from using purely NOR gates.

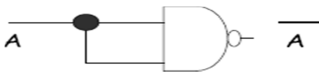
NAND Gate

In this case the circuit of the AND gate is fed to the input of an inverter. The gate gives an output of 1 if either A or B or both are 0. The NAND gate is also a universal gate as it can be construed as shown to get either an AND gate or an OR gate operation. The NAND gate symbol is an AND gate symbol with a bubble at the output pin as shown below.

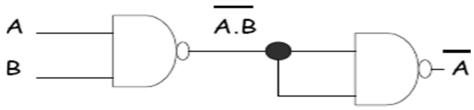
$C = A.B$

A	B	C
0	0	1
0	1	0
1	0	1
1	1	0

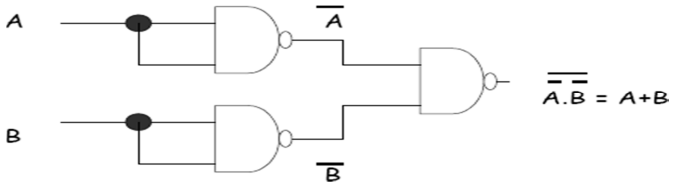
Implementation of a NOT gate using a NAND



Implementation of an AND gate using a NAND

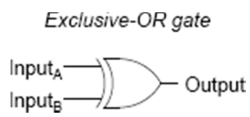


Implementation of an OR gate using a NAND



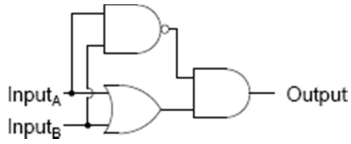
XOR Gate

Exclusive-OR gates output a high, (1) logic level if the inputs are at different logic levels, either 0 and 1 or 1 and 0. Conversely, they output a low (0) logic level if the inputs are at the same logic levels. The Exclusive-OR (sometimes called XOR) gate has both a symbol and a truth table pattern shown below:



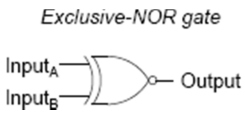
A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

There are equivalent circuits for an Exclusive-OR gate made up of AND, OR, and NOT gates, just as there were for NAND and NOR gates. A rather direct approach to simulating an Exclusive-OR gate is to start with a regular OR gate, then add additional gates to inhibit the output from going, high, (1) when both inputs are high. (1):



3.8 XNOR Gate

Exclusive-NOR gate, otherwise known as the XNOR is equivalent to an Exclusive-OR gate but it has an inverted output. The truth table for this gate is exactly opposite as for the Exclusive-OR gate:



A	B	Output
0	0	1
0	1	0
1	0	0
1	1	1

Example 1

A digital signal 101011 is applied to a NOT gate what will be the NOT gate output.

Input = 1 0 1 0 1 1

Output = 0 1 0 1 0 0

SELF ASSESSMENT EXERCISE

Two signals A = 1 0 1 1 0 1 and B = 1 1 0 1 0 1 are fed to a 2 input AND gate sketch the output signal.

Convert the following Boolean expression to logic using different logic gates.
(A. B + C)

4.0 CONCLUSION

In this unit you have been introduced to the different logic gates, their symbols and applications.

5.0 SUMMARY

In this unit we have been able to extend knowledge of the theory and applications of the different types of logic gates.

6.0 TUTOR-MARKED ASSIGNMENT

Two signals A = 1 0 1 1 0 1 and B = 1 1 0 1 0 1 are fed to a 2 input AND gate sketch the output signal.

Using DeMorgan's theorem, convert the following Boolean expressions to equivalent expressions that (i) have only OR and complement operations, and show that the functions can be implemented with NOR gates only; (ii) have only AND and complement operations, and show that the functions can be implemented with NAND gates only.

(a)
(b) _

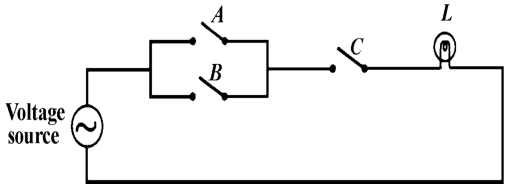
_ _
f □ x y □
f □ (y □

_
xz □

_
z)(x □
yz

_
y)(y □ z)

3) Express the switching circuit shown in the figure in binary logic notation and generate the truth table



7.0 REFERENCES/FURTHER READING

Fitchen F.C; (1972). Transistor Circuit Analysis and Design. Second Edition Van Nostrand Reinhold Publishers.

Maddock R.J and Calcutt D.M (1994). Electronics: a Course for Engineers Second Edition. Longman Publishers.

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UNIT 3 KARNAUGH MAPS AND LOGIC CIRCUIT SIMPLIFICATION

CONTENTS

1.0 INTRODUCTION

In the design of logic functions by means of logic gates, more than one solution is usually available for the implementation of a given logic expression and some combinations of gates can implement a given function more efficiently than others. The challenge in logic design is the assurance of having chosen the most efficient realization.

A very popular and easy to use procedure for simplifying logic design exists and it utilizes a map, describing all possible combinations of the variables present in the logic function of interest. This map is called a Karnaugh map, after its inventor. The karnaugh map consists of row and column assignments for two or more variables arranged so that all adjacent terms change by only one bit. Each map consists of 2N cells, where N is the number of logic variables. Karnaugh maps allow us to convert a truth table to a simplified Boolean expression without using Boolean Algebra.

2.0 OBJECTIVES

At the end of this unit, student should be able to:

- the understanding of the use of karnaugh maps in logic design
- the understanding of the use of karnaugh maps in simplification of logic design
- the understanding of conversion of truth tables to Boolean algebra
- the generation of digital logic circuits from truth tables.

3.0 MAIN CONTENT

3.1 Introduction to Karnaugh Maps

Karnaugh maps are a graphical way of simplifying a Boolean expression and thus simplifying the resulting circuit. A Karnaugh map is a completely mechanical method of performing this simplification, and so has an advantage over manipulation of expressions using Boolean algebra. Karnaugh maps are effective for expressions of up to about six variables. For more complex expressions the more advanced Quine-McKluskey method may be appropriate.

The Karnaugh map uses a rectangle divided into rows and columns in such a way that any product term in the expression to be simplified can be represented as the intersection of a row and a column. The rows and columns are labeled with each term in the expression and its complement. The labels must be arranged so that each horizontal or vertical move changes the state of one and only one variable. The figure 3.1 below shows karnaugh map with 2,3and 4 variables

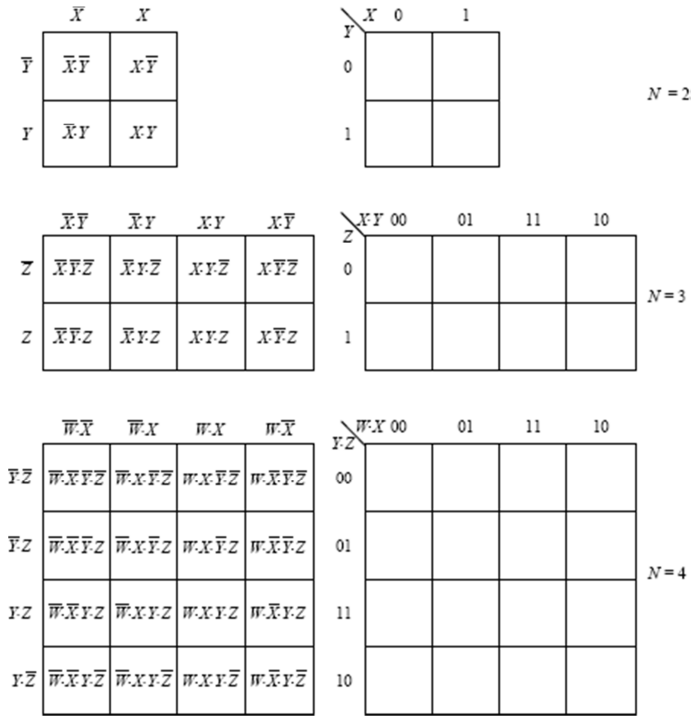


Figure 3.1 Karnaugh maps with 2, 3, 4 variables

3.2 Circuit Simplification Using Karnaugh Maps

The following steps are required to use a Karnaugh map to simplify an expression:

Draw a “map” with one box for each possible product term in the expression.

The boxes must be arranged so that a one-box movement either horizontal or vertical changes one and only one variable. See Figure 3.1.
For each product term in the expression to be simplified, place a checkmark (or a 1) in the box whose labels are the product's variables and their complements.

Draw loops around adjacent pairs of checkmarks. Blocks are “adjacent” horizontally and vertically only, not diagonally. A block may be “in” more than one loop, and a single loop may span multiple rows, multiple columns, or both, so long as the number of checkmarks enclosed is a power of two.

For each loop, write an unduplicated list of the terms which appear; i.e. no matter how many times A appears, write down only one A.
If a term and its complement both appear in the list, e.g. both A and $\bar{A}$ delete both from the list.

For each list, write the Boolean product of the remaining terms.
Write the Boolean sum of the products from Step 5; this is the simplified expression.

Example 1

Simplify the Boolean expression below using karnaugh maps AB A B
Solution

This is an expression of two variables. A rectangle is drawn and divided so that there is a row or column for each variable and its complement. Next, we place checks in the boxes that represent each of the product terms of the expression.

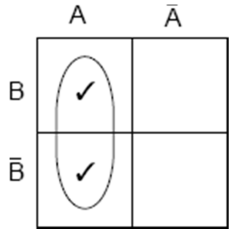


Figure 3.2: Karnaugh map for example 1

The first product term is AB, so a check is placed in the upper left block of the diagram, the conjunction of A and B.
The second is A B , so we place a check in the lower left block. Finally, we draw a loop around adjacent pairs of checks. The loop contains A, B,

A, and B . We remove one A so that the list is unduplicated. The B and B "cancel," leaving only A, which is the expected result: AB□ AB □ A.

Example 2

Simplify A B □ A B □

AB using K-Maps

Solution
There are two variables, so the K-Map is the same as in Example 1. The solution will be derived using the following steps:
Place a check in the A B area. Place a check in the A B area.
Place a check in the AB area.

Draw loops around pairs of adjacent checks.

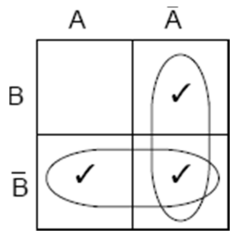


Figure 3.3: Karnaugh map for example 2

The Vertical loop contains A , B, A, B . Since A is duplicated, one of it is removed. B and its complement B both cancel out leaving only A .

From the horizontal loop we have A, B , A, B .The duplicate B is removed and the A cancels out with its complement.
The Boolean sum of the manipulation is now A + B which is the answer.

3.3 Simplifying Logic Circuits Using Karnaugh Maps

The major advantage of Karnaugh maps is its ability to simplify logic design by simplifying the Boolean expression and/or truth table and eliminating unnecessary logic gates in a digital logic design.

Example 3

Given the truth table for a 3 input logic design:
Generate the Boolean equation and sketch the logic circuit required to implement the truth table

Simplify the logic design using K-maps and sketch the resultant logic circuit.

The output is the X column.

Table 3.2 Output of the 3 input logic circuit

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Solution

From the truth table, the circuit generates an output when X = 1.The product of the terms at which X = 1 is taken out and summed together. This sum is known as sum of products and it is the Boolean expression that generates the truth table.

Products terms are:

$A\bar{B}C$,

$\bar{A}\bar{B}\bar{C}$

and $AB\bar{C}$

Sum of products =

$\bar{A}\bar{B}\bar{C}$

+ $A\bar{B}C$

+ $AB\bar{C}$

The digital logic circuit based on the Boolean equation is given below. Note, the inputs are A, B and C and the complements are

$\bar{A}\bar{B}\bar{C}$

The complements are generated by the use of inverters or NOT gates. $A\bar{B}C$ complements are fed into a 3 input AND gate while $AB\bar{C}$ is fed into another 3 input AND gate and $\bar{A}\bar{B}\bar{C}$ is fed into the third 3 input AND gate. The inputs of the three 3-input AND gates are fed together into a 3-input OR gate. The circuit diagram is shown below.

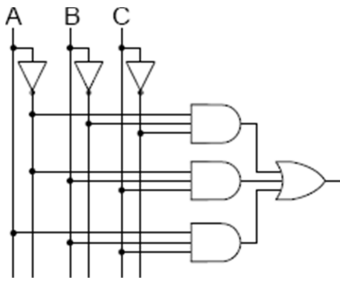


Figure 3.4: Digital logic circuit for example 3

The truth table generates an expression with three product terms. A measure of the complexity of a digital logic circuit is the number of gate inputs. The circuit in

Figure 9.4 has 15 gate inputs. The Karnaugh map for the sum of products expression is shown in Figure 9.5 below.

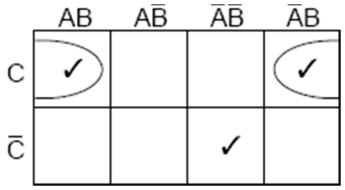


Figure 3.5 Karnaugh map for example 3

In this Karnaugh map, the large loop surrounds A B C and ABC .It "wraps around" from the left edge of the map to the right edge. The A and A cancel, so these two terms simplify to BC.

$\bar{A}\bar{B}\bar{C}$
is in a cell all by itself, and so contributes all three of its terms to the final expression.

The simplified expression is B C □ ABC and the simplified circuit is shown in Figure 9.6. In the simplified circuit, one three-input AND gate was removed, a remaining AND gate was changed to two inputs, and the OR gate was changed to two inputs, resulting in a circuit with ten gate inputs.

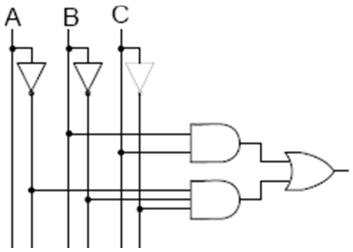


Figure 3.6: Simplified Circuit in example 3

4.0 CONCLUSION

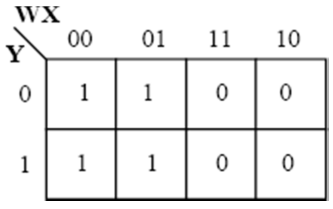
In this unit you have been introduced to the use of the karnaugh map in simplification of digital logic circuits. The following observations are to be noted in the generation of loops in the K-maps. For maximum simplification, the loops are to be made as big as possible with big loops being the preferred size. The restriction is that the loop must be rectangular and enclose a number of checkmarks that is a power of two. When a map is more than two rows deep, i.e. when it represents more than three variables, the top and bottom edges can be considered to be adjacent in the same way that the right and left edges are adjacent in the two-by-four maps above. If all checkmarks in a loop are enclosed within other loops as well, that loop can be ignored because all its terms are accounted for.

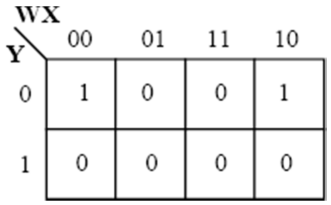
5.0 SUMMARY

In this unit we have been able to extend knowledge of the theory and applications of the Karnaugh Maps.

6.0 TUTOR-MARKED ASSIGNMENT

1 Given the following Karnaugh maps, determine their logic equation.





Given the truth table for a 3 input logic design,
Generate the Boolean equation and sketch the logic circuit required to implement the truth table in Table 9.3
Simplify the logic design using K-maps and sketch the resultant logic circuit.

The output is the X column.

Table 3.3 Output of the 3 input logic circuit

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1

1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

3 Use a Karnaugh map to simplify A B C □ A BC □ −− ___ $\overline{ABC}$.

7.0 REFERENCES/FURTHER READING

Mendelson, Elliott, (1970). Schaum's Outline of Theory and Problems of Boolean Algebra. McGraw- Hill

Maddock R.J and Calcutt D.M (1994). Electronics: a Course for Engineers Second Edition. Longman Publishers.

Neamen D.A (1996). Electronics Circuit Analysis and Design.

McGraw-Hill Publishers.

UNIT 4 COMBINATIONAL CIRCUITS – ARITHMETIC & LOGIC FUNCTIONS: ADDERS, SUBTRACTORS, COMPARATORS

CONTENTS

1.0 INTRODUCTION

This unit is designed to equip the student with a proper understanding of how arithmetic & logic functions are obtained via combinational circuits. The unit focuses on fundamental arithmetic functions i.e. adders, subtractors, and comparators.

2.0 INTENDED LEARNING OUTCOMES (ILOS)

The student is expected at the end of this unit to be able to have a good understanding of how combination circuits can be used to realize arithmetic & logic functions that are central to the operation of microprocessors.

3.0 MAIN CONTENT

3.1 Adders

There are fundamentally two types of adders from which other types of adders are derived. These include half adder, and the full adder, and the operation of each type of adder is governed by a truth table. The following sub-sections discusses these adders.

3.1.1 Half Adder

The half adder as a combinational circuit is used for the addition of two bits. The circuit for this type of adder is characterized by two inputs, and two outputs. The input bits are called augend and addend bits, while the output bits are called sum and carry bits. Figure 3.1 shows the circuit

diagram for the half adder while Table 3.1 shows its corresponding truth table.

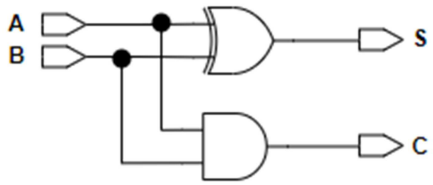


Figure 3.1: Half adder circuit

Table 3.1: Half adder truth table

Inputs		Outputs	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

From the circuit diagram, the logic equation for the half adder can be deduced as follows:

$$S = A \oplus B$$
$$C = AB \qquad (3.1)$$

The validation of the logic equation 3.1 using VHDL hardware description is shown in figure 3.2.

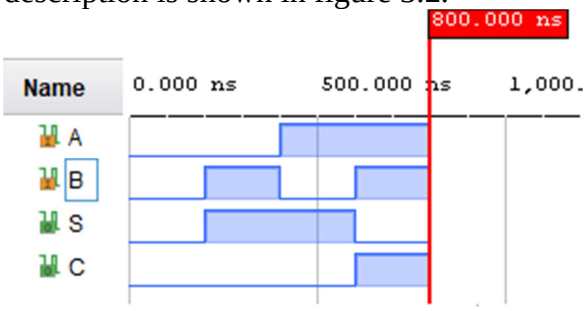


Figure 3.2: Digital waveform validation of half adder using VHDL

3.1.2 Full Adder

The full adder is used for the addition of three input bits where the first bit represents the augend, the second the addend, and the third the carry

bit from a previous addition. Similar to the half adder, it has two outputs- the sum output, and the carry output. Figure 3.3 shows the circuit diagram for the full adder, while Table 3.2 shows its corresponding truth table.

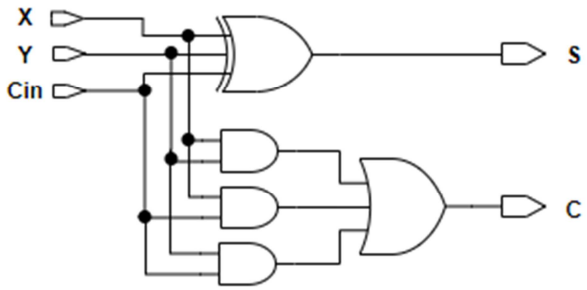


Figure 3.3: Full adder circuit

Table 3.2: Full adder truth table

Inputs			Outputs	
X	Y	Cin	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

From the circuit diagram, the logic equation for the full adder can be deduced as follows:

$$S = X \oplus Y \oplus C_{in}$$
$$C = XY + XC_{in} + YC_{in} \quad (3.2)$$

The validation of the logic equation 3.2 using VHDL hardware description is shown in figure 3.4.

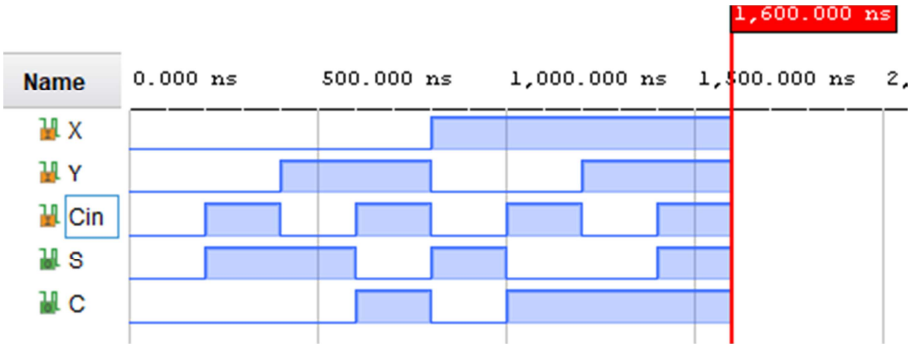


Figure 3.4: Digital waveform validation of half adder using VHDL

3.2 Subtractors

Similar to adders, there are fundamentally two types of subtractors- half subtractor, and full subtractor. Other types of subtractors are derived from these two.

3.2.1 Half Subtractors

The half subtractor is similar to the half adder in the sense it has two inputs and two outputs. It subtracts one bit from another bit, with the first bit being the minuend bit, and the second bit being the subtrahend bit. The output bits are the difference and borrow bits. Figure 3.5 shows the circuit diagram for the half subtractor, and Table 3.3 shows its corresponding truth table.

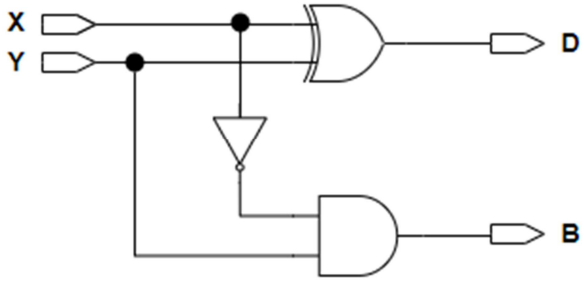


Figure 3.5: Half subtractor circuit

Table 3.3: Half subtractor truth table

Inputs		Outputs	
X	Y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

From Table 3.3, equation 3.3 is derived for the half-subtractor.

$$D = X \oplus Y$$
$$B = \bar{X}Y \qquad (3.3)$$

The functional verification of the Table 3.3 is shown in figure 3.6 using digital waveforms obtained via VHDL modeling and simulation.

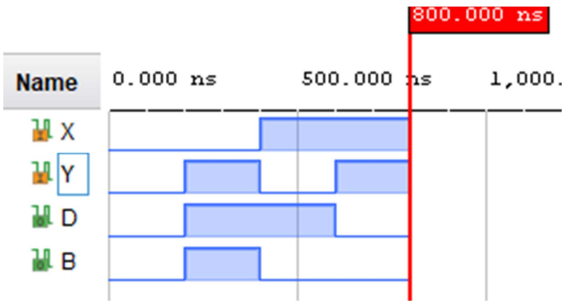


Figure 3.6: Functional verification of half subtractor truth table

3.2.2 Full Subtractors

The full subtractor is characterized by three input bits- the minuend, the subtrahend, and the borrow bit from a previous level of operations. Similar to the half subtractor, it also has two outputs- the difference D, and the present borrow B. Figure 3.7 shows the circuit for the full subtractor, while Table 3.4 shows the truth table for the circuit.

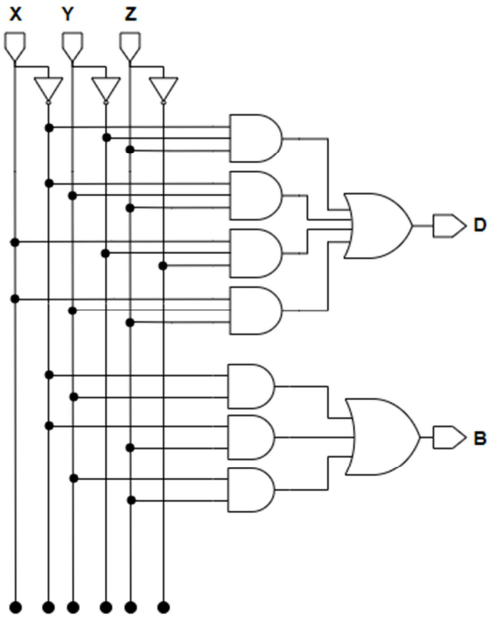


Figure 3.7: Full subtractor circuit

Table 3.4: Truth table for full subtractor

Inputs			Outputs	
X	Y	Z	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

From the circuit diagram and the truth table, the logic equation for the full subtractor is derived as shown in equation 3.4, while the validation of the truth table is shown in figure 3.8 using digital waveform analysis.

$$D = \bar{X}\bar{Y}Z + \bar{X}Y\bar{Z} + X\bar{Y}\bar{Z} + XYZ$$
$$B = \bar{X}Y + \bar{X}Z + YZ \qquad (3.4)$$

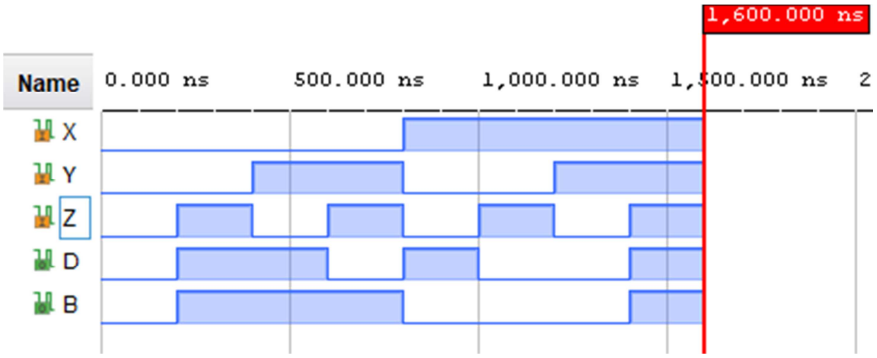


Figure 3.8: Functional verification of full subtractor truth table

3.2 Comparators

A comparator is a combinational circuit that compares two binary numbers and determines the relationship between them as being equal, less than, or greater than. In practice, the most widely used comparator is the magnitude comparator. Given two binary numbers A and B, the operation of the magnitude comparator on these two numbers outputs one of three possibilities i.e. A = B, A < B, or A > B.

To understand the working of the magnitude comparator, consider an example when both A and B are 4-bits wide as follows A = A3A2A1A0, and B = B3B2B1B0. The two numbers are equal when A3 = B3, A2 = B2, A1 = B1, and A0 = B0; this comparison is determined by the relationship in equation (3.5).

$$x_i = A_i B_i + A_i^i B_i^i \qquad (3.5)$$

where xi = 1 iff the ith bits are equal.

Consequently for the 4-bit comparator, $(A = B) = (x_3x_2x_1x_0)$

$$(A > B) = A_3B_3' + x_3A_2B_2' + x_3x_2A_1B_1' + x_3x_2x_1A_0B_0'$$

$$(A < B) = A_3'B_3 + x_3A_2'B_2 + x_3x_2A_1'B_1 + x_3x_2x_1A_0'B_0$$

The gate level implementation for the three outputs i.e. A = B, A > B, and A < B is shown in figure 3.9.

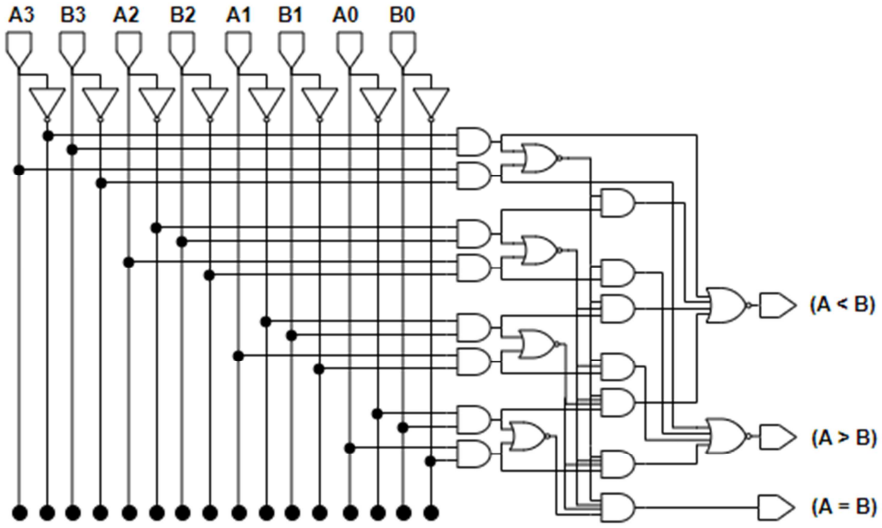


Figure 3.9: Combinational circuit for a 4-bit magnitude comparator

The simulation of the circuit using VHDL yields the waveform function verification of the circuit as shown in figure 3.10.

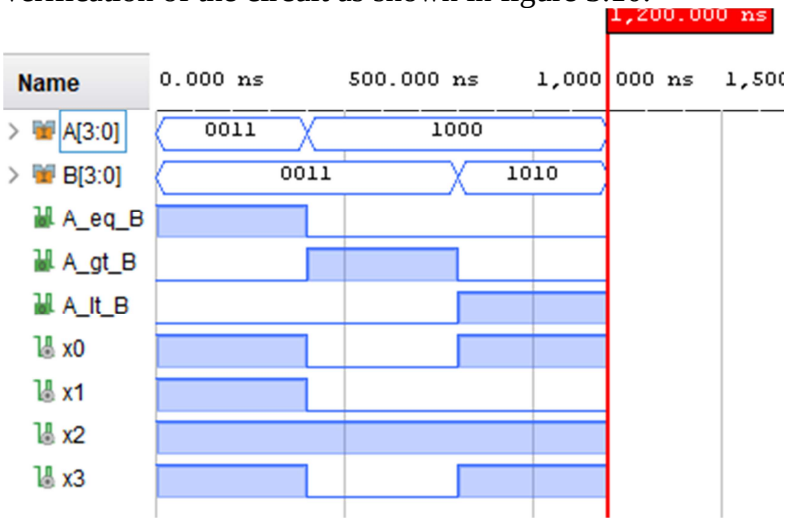
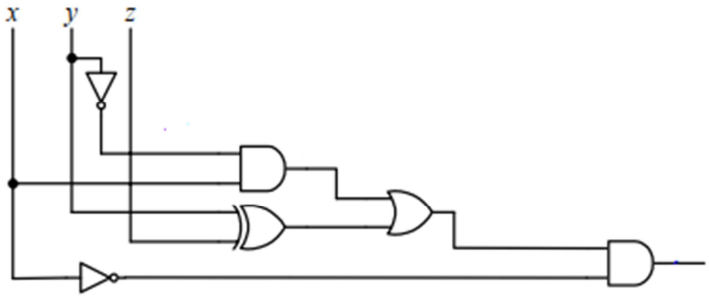


Figure 3.10: Functional verification of 4-bit magnitude comparator

4.0 TUTOR MARKED ASSIGNMENT

Consider the combinational circuit shown below:



Derive the logic equation for the circuit, and from the equation, construct a corresponding truth table.

5.0 CONCLUSION

In this unit, you have been introduced to the three most fundamental arithmetic & logic circuits i.e. adders, subtractors, and comparators as combinational circuits. You have also been shown the nexus between a truth table and the behavior of a combinational circuit.

6.0 SUMMARY

The unit has been able to show to the reader how the theoretical knowledge of a class of combinational circuit is used in realizing arithmetic & logic functions. The reader has also been shown the central role truth tables play in understanding and using combinational circuits.

7.0 REFERENCES/FURTHER READING

Tertulien, N. (2016). Digital Electronics1: Combinational Logic Circuits. Wiley, pp 1 – 276. ISBN: 978-1-848-21984-7

UNIT 5 COMBINATIONAL CIRCUITS – DATA TRANSMISSION: MULTIPLEXERS, DEMULTIPLEXERS, DECODERS, ENCODERS

CONTENTS

1.0 INTRODUCTION

This unit is designed to equip the student with a proper understanding of how data transmission systems are designed via combinational circuits. The unit focuses on combinational circuit components that are central to the success of data transmission circuits.

2.0 INTENDED LEARNING OUTCOMES (ILOS)

The student is expected at the end of this unit to be able to have a good understanding of how combination circuits can be used to in the design of data components that used in the design of data transmission systems.

3.0 MAIN CONTENT

3.1 Multiplexers

Multiplexers are a special class of combinational circuits that are characterized by a single output, and allow the passage of a particular binary information to the output from a set of possible inputs; the selection of the binary input is done by a set selection lines whose combination enables the input of interest to be passed to the output. For any set of 2n input lines in a multiplexer, there are n selection lines. Conceptually, figure 3.1 shows how a multiplexer is typically represented in a digital circuit design.

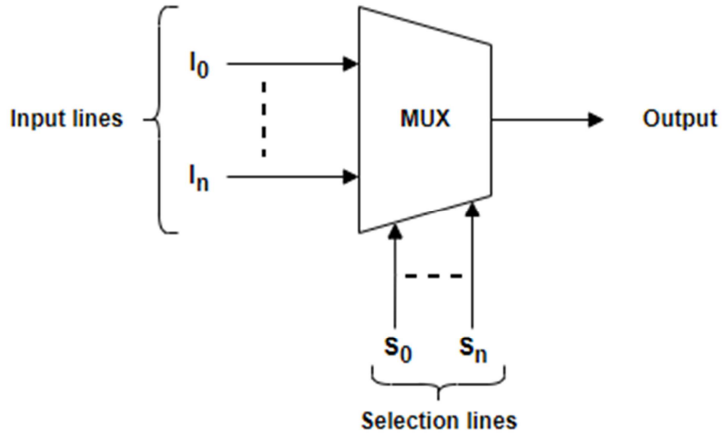


Figure 3.1: Block diagram of a multiplexer

Consider the case of a 4-to-1 multiplexer i.e. 4-inputs 1-output multiplexer as an example. Such a circuit and its corresponding truth table are shown in figure 3.2 and Table 3.1 respectively.

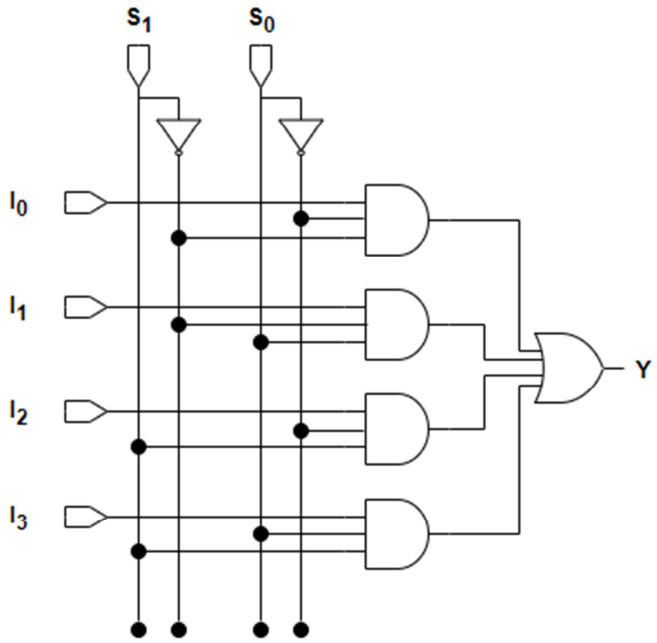


Figure 3.2: A 4-to-1 multiplexer

Table 3.1: Truth table for a 4-to-1 multiplexer

S1	S0	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

Table 3.1 shows the required selection line combination to enable an input pass to the circuit. The selection line combination that enables a particular input to be transmitted to the output also disables all other inputs from being transmitted to the output. Figure 3.3 shows the functional verification of the 4-to-1 multiplexer via VHDL modeling and simulation.

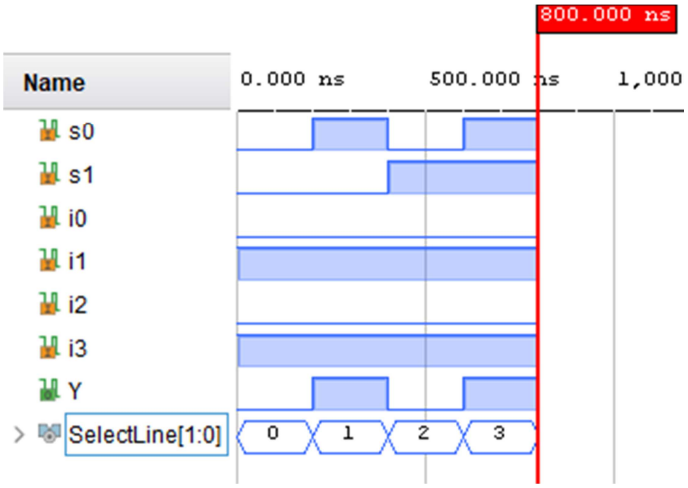


Figure 3.3: Functional verification of 4-to-1 multiplexer

3.2 Demultiplexers

Demultiplexers (demux) perform a reversal operation of multiplexers where a single input is routed to any of the members of a given set of outputs. Figure 3.4 shows the conceptual representation of a demux in a typical circuit design.

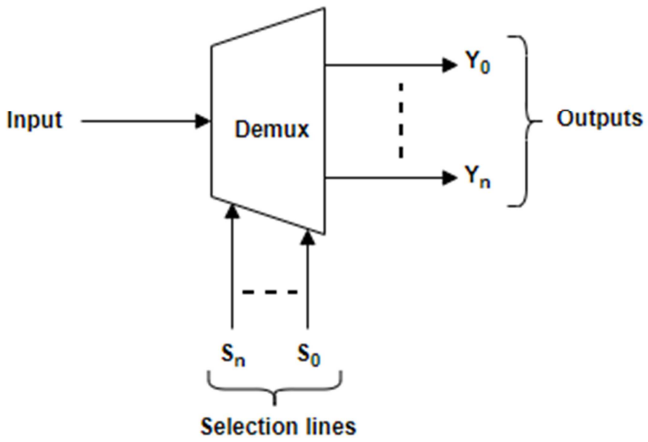


Figure 3.4: Block diagram of a demux

Consider the case of a 1-to-4 demux shown in figure 3.5, and whose truth table is shown in Table 3.2. It can be seen the routing of the input to a specific output port is achieved by the AND operation in the truth table.

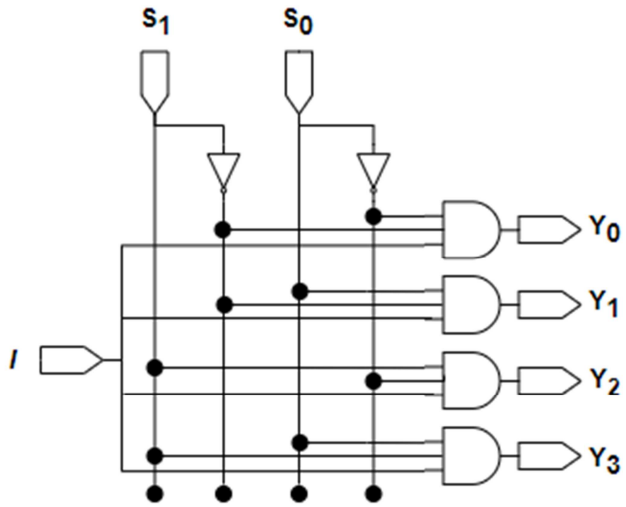


Figure 3.5: A 1-to-4 demux

Table 3.2: Truth table for a 1-to-4 demux

Selection lines		Outputs			
S1	S0	Y0	Y1	Y2	Y3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

The functional verification of the truth table is shown in figure 3.6 where the routing of the input to different outputs can be seen when the signal values in the select lines are changed.

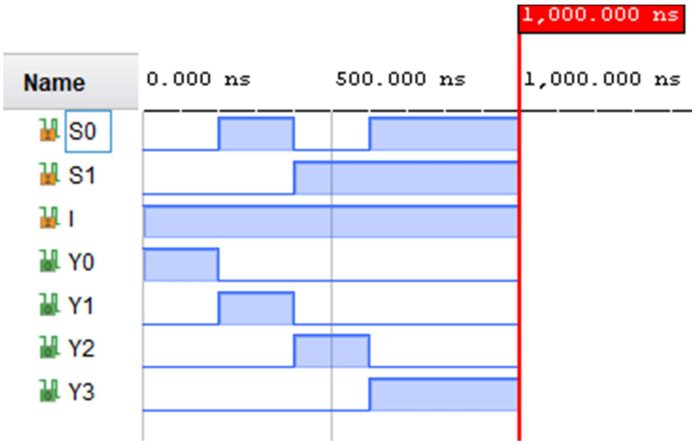


Figure 3.6: Functional verification of 1-to-4 demux

3.3 Decoders

Decoders are a class of combinational circuits that convert binary information from n input lines to a maximum of 2n output lines. The goal of decoders is to minterms that less-than-or-equal 2n for n input variables. The operation of a decoder is such that for every input combination, a unique output is asserted. Figure 3.7 shows the block diagram of a decoder.

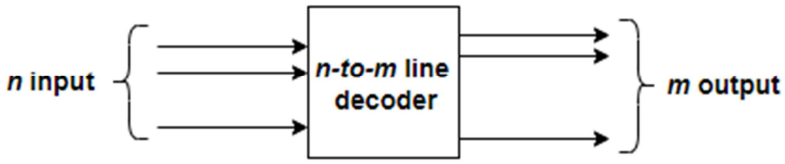


Figure 3.7: Block diagram of an n-to-m decoder

Consider the case of a 2-to-4 decoder whose circuit diagram is shown in figure 3.8, and whose truth table is shown in Table 3.3. It can be observed from the truth table that for every set of input combination, a unique set of output is generated.

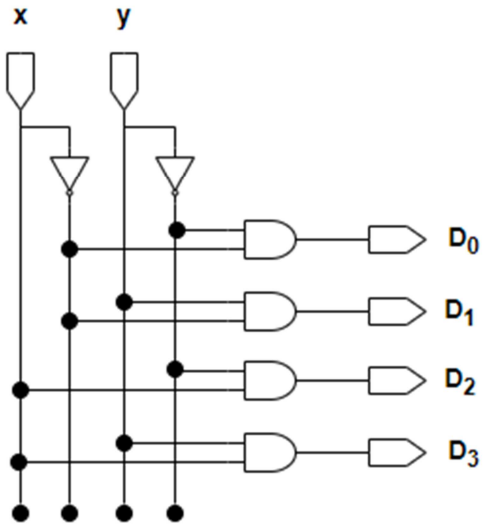


Figure 3.8: Circuit diagram of a 2-to-4 decoder

Table 3.3: Truth table of a 2-to-4 decoder

Inputs		Outputs			
x	y	D0	D1	D2	D3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

The functional of Table 3.3 via waveform analysis is shown in figure 3.9 that was generated using VHDL.

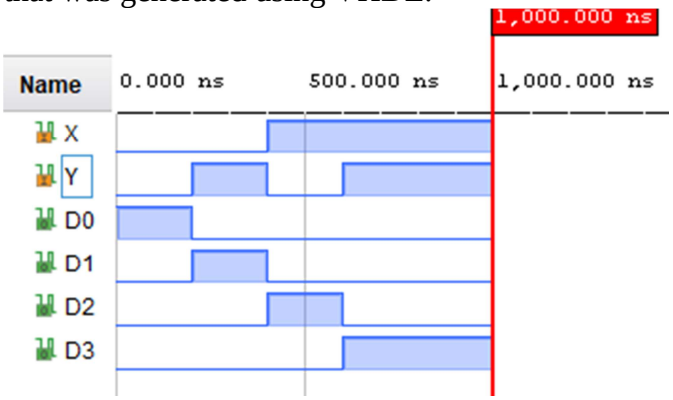


Figure 3.9: Functional verification of a 2-to-4 decoder

3.4 Encoders

Encoders are combinational circuits that perform the inverse operation of a decoder. They have less-than-or-equal to 2n input lines and n output lines. For every given input, the encoder generates a corresponding binary code on the output lines. Figure 3.10 shows the block diagram representation of an encoder.

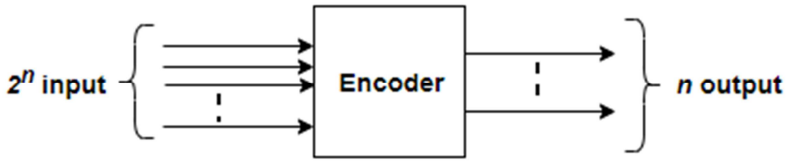


Figure 3.10: Block diagram of an encoder

A special class of an encoder is called a priority encoder whose operation is such that when two or more inputs are equal to 1 concurrently, the input with the highest priority will take precedence. Consider the case of a four input priority encoder whose circuit diagram is shown in figure 3.11, and whose truth table is shown in Table 3.4.

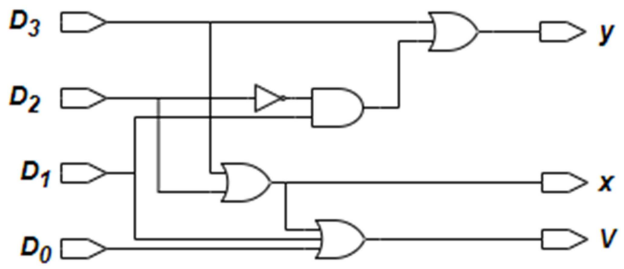


Figure 3.11: Circuit diagram of 4-input priority encoder

Table 3.4: Truth table for a 4-input priority encoder

Inputs				Outputs		
D0	D1	D2	D3	x	y	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

Table 3.4 shows a proportional relationship between the subscript number and the priority of the input, with D3 having the highest priority and D0 having the least priority.

The logical equations for the 4-input priority encoder from the circuit in figure 3.11 are stated as follows:

$$\begin{aligned} \boldsymbol{x} &= \boldsymbol{D_2} + \boldsymbol{D_3} \\ \boldsymbol{y} &= \boldsymbol{D_3} + \boldsymbol{D_1 D_2'} \\ \boldsymbol{V} &= \boldsymbol{D_0} + \boldsymbol{D_1} + \boldsymbol{D_2} + \boldsymbol{D_3} \end{aligned} \qquad (3.1)$$

The functional verification of the circuit in figure 3.11 and equation 3.1 is shown in figure 3.12, where for every possible input combination, the circuit responded according to the entries in Table 3.4.

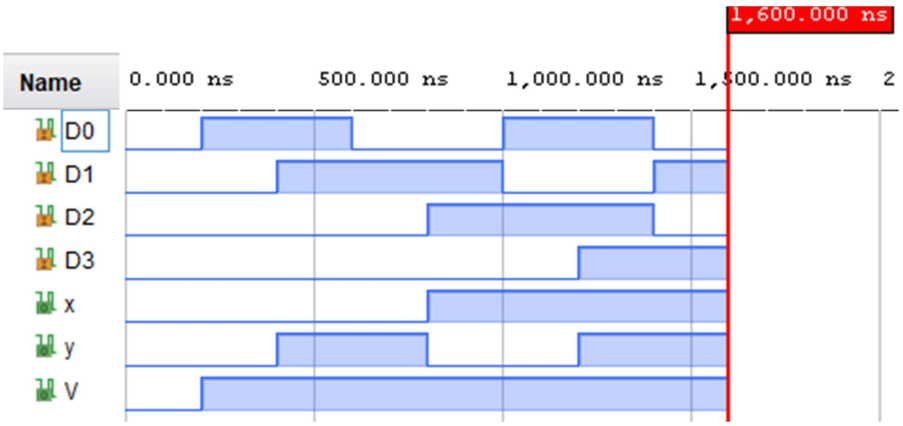


Figure 3.6: Functional verification of 4-input priority encoder

4.0 TUTOR MARKED ASSIGNMENT

The truth table for an octal-to-binary encoder is shown below:

Inputs								Outputs		
D0	D1	D2	D3	D4	D5	D6	D7	x	y	Z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Derive the logic equations for the encoder from this table, and draw the corresponding schematic from the equations.

5.0 CONCLUSION

In this unit, you have been introduced to the combinational circuits that are central to the operational of data transmission. You have been shown how truth tables are absolutely tangential to the understanding of these circuits.

6.0 SUMMARY

The unit has been able to show to the reader how the theoretical knowledge of a class of combinational circuit is used in realizing and understanding of the application of combinational circuits and their role in data transmission systems.

7.0 REFERENCES/FURTHER READING

Tertulien, N. (2016). Digital Electronics1: Combinational Logic Circuits. Wiley, pp 1 – 276. ISBN: 978-1-848-21984-7

MODULE 4 SEQUENTIAL CIRCUITS

MODULE INTRODUCTION

The module is designed to make the student develop important skills in the design and analysis of sequential circuits. It introduces the fundamental devices used in the realization of sequential circuits, and then takes the student further to the application of the devices in design examples. The unit also shows the student the standard methodology used in designing sequential based on state machines i.e. finite state machines, and algorithmic state machines.

Unit 1 Sequential circuits – Synchronous: flip-flops, registers, counters
Unit 2 Sequential circuits – Asynchronous: standard design procedure, un-clocked flip-flops, time-delay elements

UNIT 1 SEQUENTIAL CIRCUITS – SYNCHRONOUS: FLIP- FLOPS, REGISTERS, COUNTERS

CONTENTS

1.0 INTRODUCTION

This unit gives the student critical information on fundamental components of a sequential circuit. The information ranges from circuit symbol of components used in sequential circuits, their truth tables, and their areas of application in the design of basic sequential circuits to the control units of microprocessors.

2.0 INTENDED LEARNING OUTCOMES (ILOS)

For this unit, the ILOs include the ability to quickly identify sequential circuit components, their truth tables, and their status as either positive-edged triggered or negative-edge triggered sequential circuit

components. Another ILO is to know when to know the fundamental difference between a register and a flip-flop, and when to apply each. The student is also expected to develop a basic understanding of how flip-flops are used in designing counters.

3.0 MAIN CONTENT

3.1 Flip-flops

Flip-flops (FFs) are circuits in digital electronics that are characterized by two stable states that can be used for the storage of data. Through the application of varying inputs, the stored data can be changed. FFs are the foundation building blocks in electronic systems that range from communication systems, control systems, and computing systems. There are four fundamental types of flip-flops used in sequential circuits- SR flip-flop, D flip-flop, JK flip-flop, and T flip-flop; of these four, the SR, D, and JK flip are the most widely used.

3.1.1 SR Flip-flop

The SR (Set-Reset) flip-flop is the most widely used flip-flop in digital designs. The operation of the SR flip-flop is such that when the S input is HIGH i.e. digital 1, the Qa output will be HIGH and the Qb output will be LOW i.e. digital 0. Figure 3.1 shows the schematic representation for the SR flip-flop.

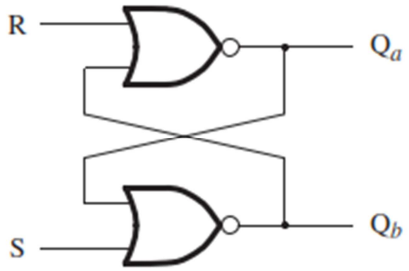


Figure 3.1: Schematic representation of an SR flip-flop

The truth table for the operation of the SR flip-flop is shown in Table 3.1 where it can be observed that when the SR inputs are both 0, there will be no change in the value at the Qa and Qb outputs of the flip-flop. When the S input is 1 and the R input is 1, the outputs of the SR are thrown into a 0 output; this can lead to unpredictable behavior in a digital system. For other possible combinations, the Qa output trails the S input, and the Qb output trails the R input. Figure 3.2 shows the digital waveform verification for the truth table SR flip-flop.

Table 3.1: The truth table of an SR flip-flop

S	R	Qa	Qb	
0	0	0/1	1/0	No change
0	1	0	1	Reset
1	0	1	0	Set
1	1	0	0	Forbidden

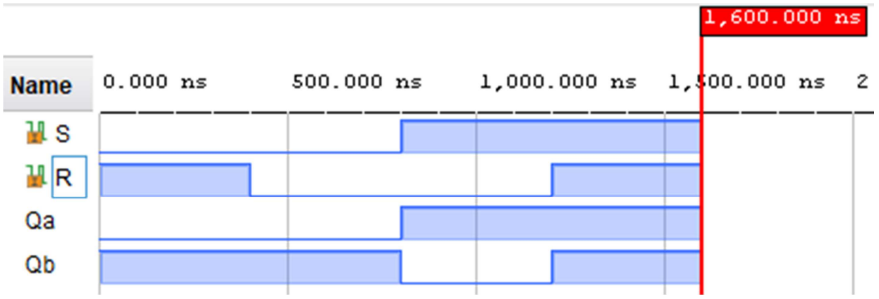


Figure 3.2: Waveform verification of the SR flip-flop

3.1.2 D Flip-flop

The D flip-flop is characterized by a single input called D input, and two outputs Qa, and Qb. The schematic for the D flip is shown in figure 3.3; it is based on the idea of the SR flip, where the S and R inputs are connected to the D input, with R input connecting through an inverter.

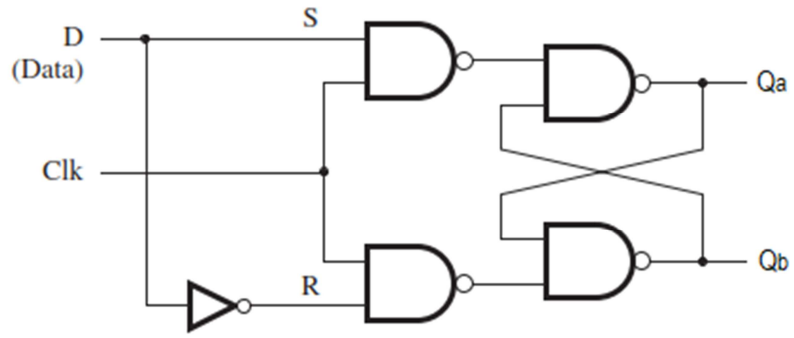


Figure 3.3: Schematic of the D flip-flop

When the D input is HIGH, S becomes HIGH and R becomes LOW; this translates in the Qa output becoming HIGH and Qb output becoming LOW at the rising edge of the Clk signal. When D is LOW, the S input becomes LOW, and the R input becomes HIGH; at the output and at the rising edge of the clock, Qa becomes LOW, and Qb becomes HIGH. Table 3.2 shows the truth table of the D flip-flop. The digital waveform verification for the truth table of the D flip-flop is shown in figure 3.4.

Table 3.2: The truth table of D flip-flop

D	Qa	Qb	
0	0	1	Reset
1	1	0	Set

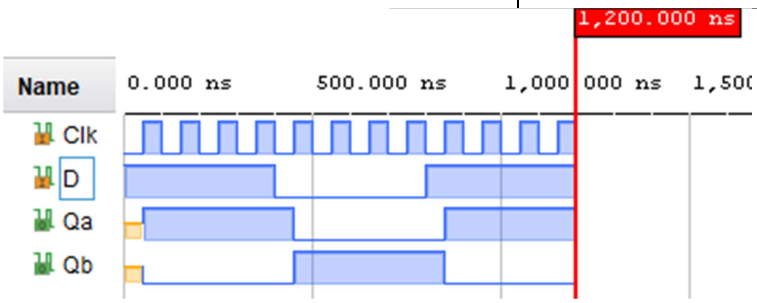


Figure 3.4: Waveform verification of the D flip-flop

3.1.3 JK Flip-flop

The JK flip-flop is a device that operates in a manner to the SR flip-flop where the function of the J input corresponds to the S input in the SR flip-flop and the K input corresponds to the R input in the SR flip-flop. The fundamental difference between the JK flip-flop and the SR flip-flop is that when the J and K inputs are HIGH, the next state of the flip-flop is the inverse of the current state; for the SR flip-flop, when S and R inputs are HIGH, its next state is undefined. Figure 3.5 shows the schematic for the JK flip-flop, and Table 3.3 shows the truth table of the JK flip-flop.

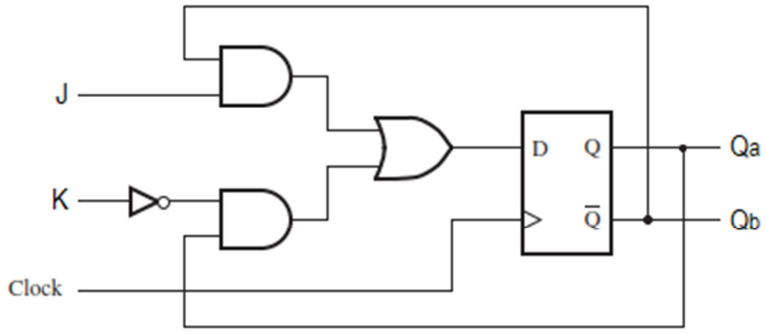


Figure 3.5: Schematic for JK flip-flop

Table 3.3: The truth table of an SR flip-flop

J	K	Qa	Qb	
0	0	Qa	Qb	No

				change
0	1	0	1	Reset
1	0	1	0	Set
1	1	Qb	Qa	Inverse

Figure 3.6 shows the verification of the truth table of the JK flip-flop using digital waveform analysis.

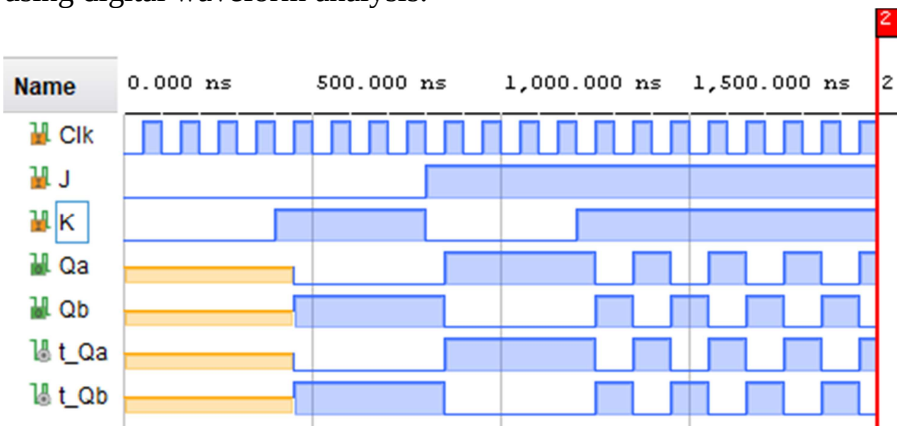


Figure 3.4: Waveform verification of the JK flip-flop

3.1.3 T Flip-flop

The T flip-flop is characterized by a single input called the T (Toggle) input similar to the D flip-flop. When T is HIGH, the output of the flip-flop toggles between 0 and 1 on the active edge of the clock signal. When it is LOW, the current state is maintained by the flip-flop. Figure 3.5 shows the schematic of the T flip-flop, and Table 3.4 shows the truth table of the flip-flop.

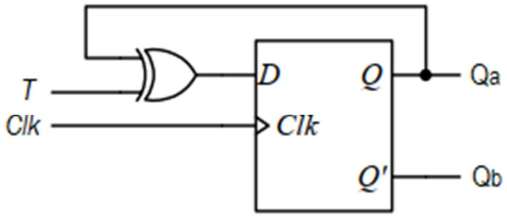


Figure 3.5: Schematic of the T flip-flop

Table 3.3: The truth table of an SR flip-flop

T	Qa	Qanext	Qbnext
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

The digital waveform for the functional verification of the truth table is shown

in figure 3.6.

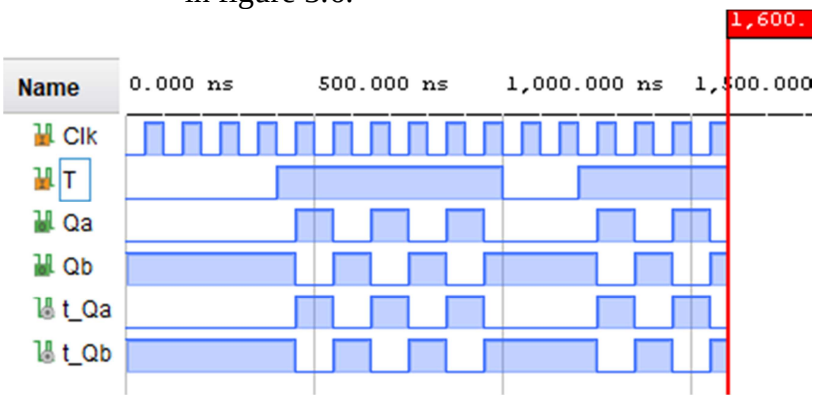


Figure 3.6: Waveform verification of the T flip-flop

3.2 Registers

Registers are n-bit structures designed for storing n-bit of information. The structure is made of n number of flip-flops (usually D flip-flops) that share a common clock, and a common clear signal. Each flip-flop in the register stores a unique bit of information. There are different types of registers in literature, some of the most notable ones include parallel load registers, and shift registers.

The parallel load registers allow the loading of all n-bits concurrently, and it equally outputs the bits concurrently. Figure 3.7 shows a typical parallel load register for a case of 4-bits. The bits get loaded concurrently from the D inputs, and are clocked out at the Q outputs. Figure 3.8 shows the functional verification of the register using digital waveform analysis.

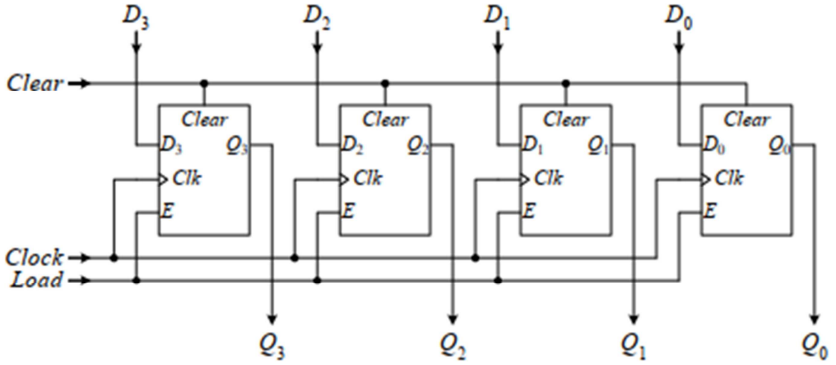


Figure 3.7: A parallel load register (4 bits)

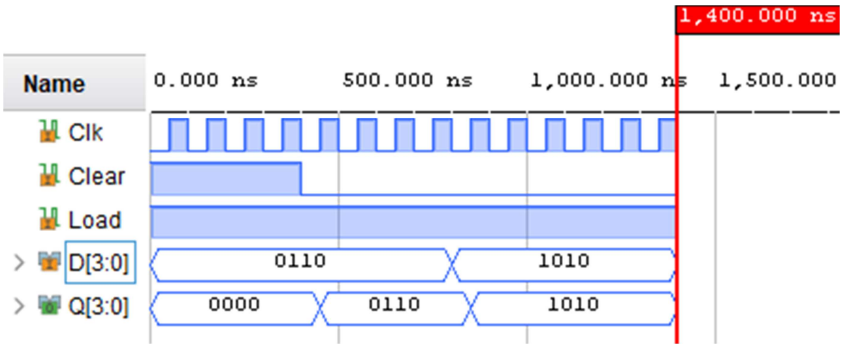


Figure 3.8: Functional behavior of a 4-bit parallel load register

Shift registers are used for shifting and rotation operations on data that are stored in the registers. Thus, they can be used for shifting a data from an input point to an output point (serial-in-serial-out shift register) passing a cascade of registers; they can also be used for conversion of a serial data input to a parallel data output and vice versa. The structure of the serial-in-serial-out (SISO) shift register is shown in figure 3.9, and figure 3.10 shows the functional verification of the register using digital waveforms.

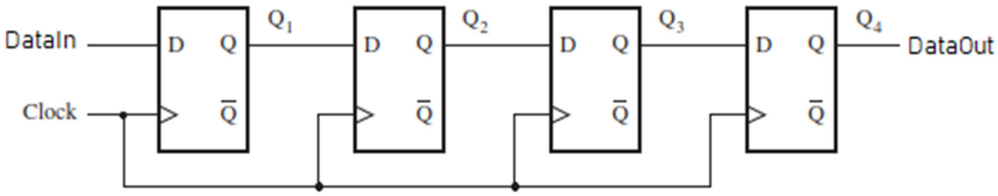


Figure 3.9: SISO shift register

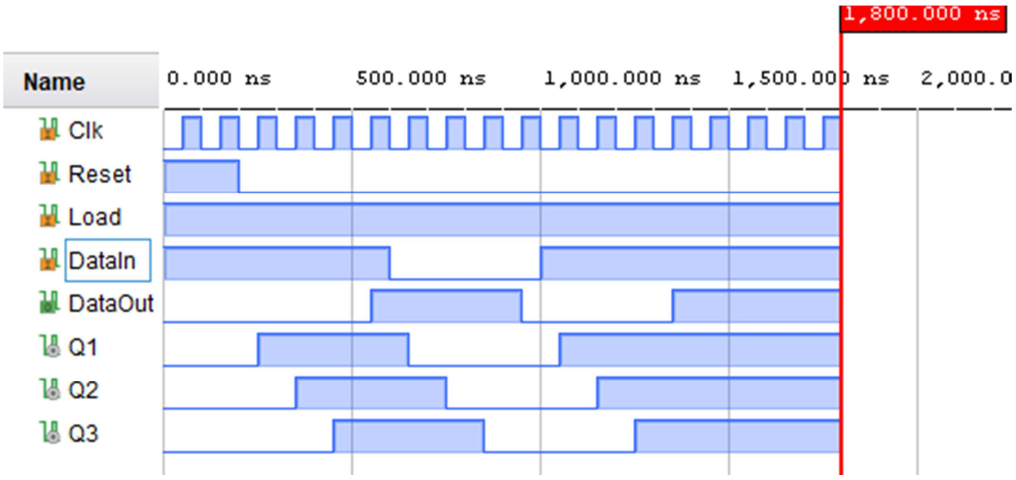


Figure 3.10: Functional behavior of a SISO register

Another type of shift register is the serial-in-parallel-out (SIPO) register. Its operation is characterized by a serial input and a parallel output. Figure 3.11 shows the structure of the register. Data enters the register via the DataIn port, and the first output i.e. Q3 receives the data after the first clock cycle; the data travels to Q2 after two clock cycles, Q1 after three clock cycles, and Q0 after four clock cycles. Figure 3.12 shows the functional behavior of the SIPO shift register using digital waveforms.

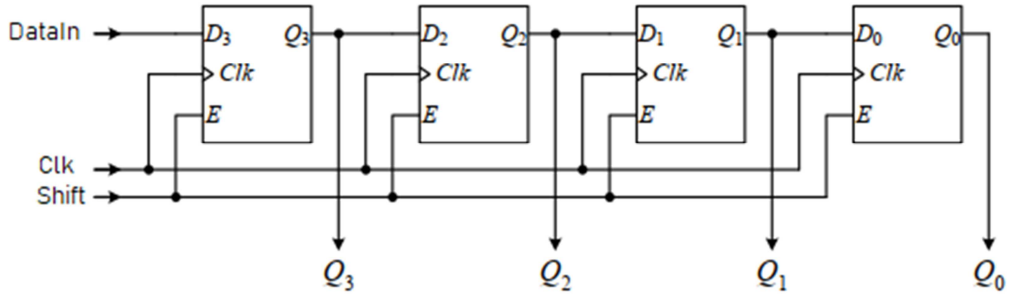


Figure 3.11: Structure of the SIPO register

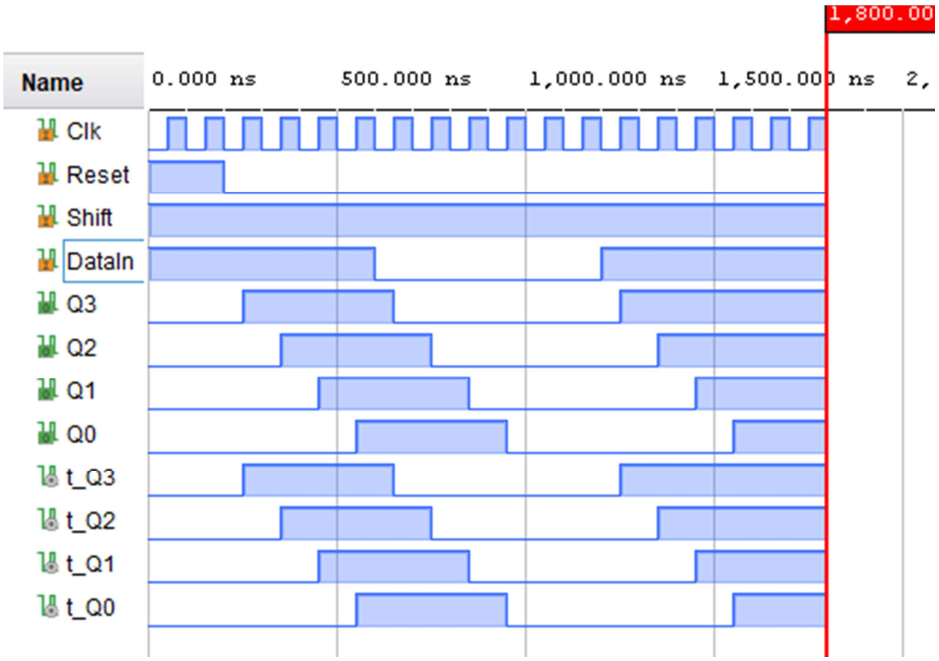


Figure 3.12: Functional behavior of the SIPO register

3.2 Counters

Counters are sequential circuits used for counting sequence of values where they measure the frequency of a given signal or the interval between two unknown time instants. Counters can be broadly divided into asynchronous, and synchronous counters.

In asynchronous counters, the clock is applied to the first flip-flop only, while the clock input to any succeeding flip-flop is derived from the output of the preceding flip-flop. Figure 3.13 shows an asynchronous counter using JK flip-flop and having n stages, while figure 3.14 shows a T flip-flop version of it having three stages. Figure 3.15 shows the function behavior of the counter based on T flip-flop.

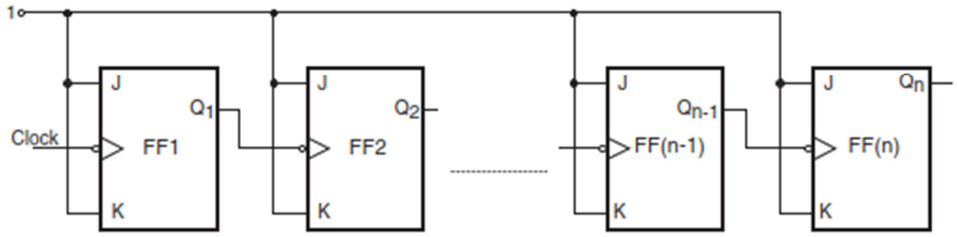


Figure 3.13: Asynchronous counter using JK flip-flop

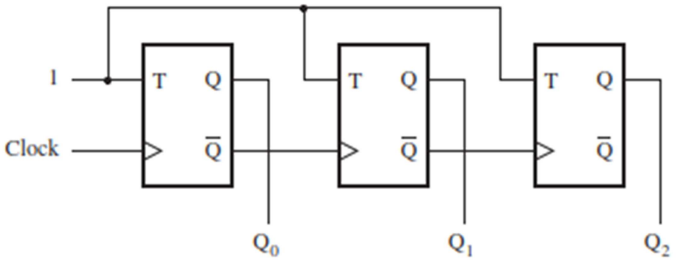


Figure 3.14: Asynchronous counter using T flip-flop

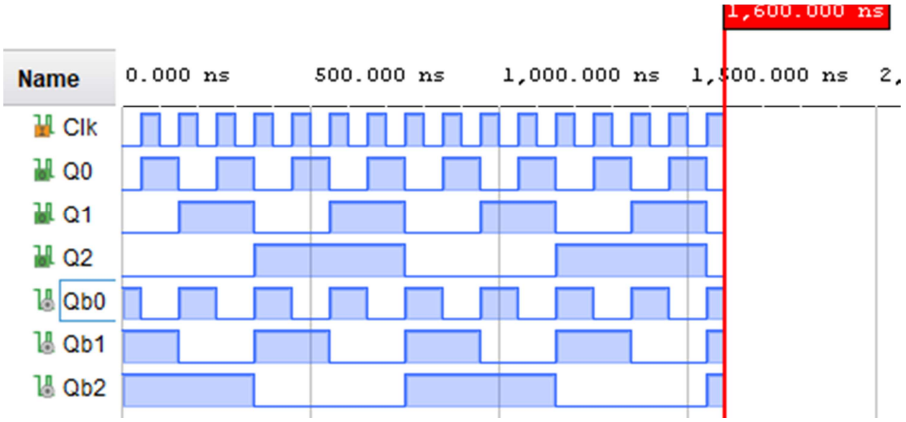


Figure 3.15: Functional behavior of T flip-flop

Synchronous counters are designed in a manner that all the flip-flops are clocked at the same time. Irrespective of the number of flip-flops involved in the construction of this counter, the propagation delay is equal to delay of only one flip-flop. Figure 3.16 shows an example of a synchronous counter that counts in the sequence 0 → 3 → 5 → 7 → 6 → 0, and whose functional behavior is shown in figure 3.17 using digital waveform analysis.

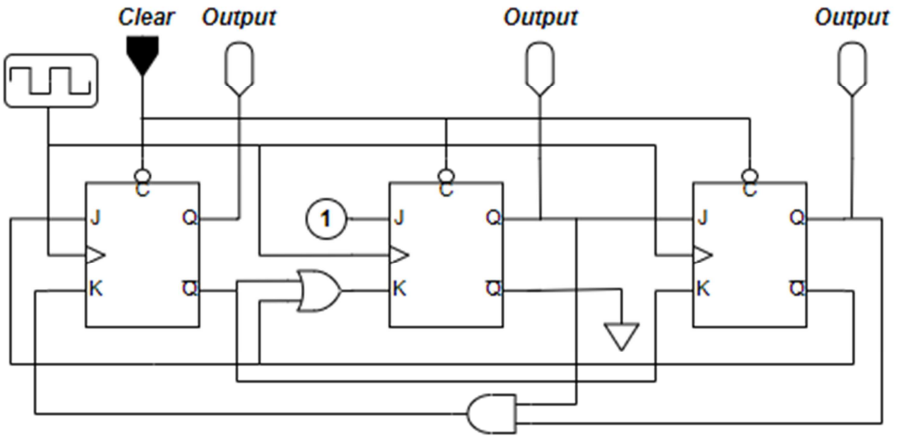


Figure 3:16: Synchronous counter to count 0 → 3 → 5 → 7 → 6 → 0

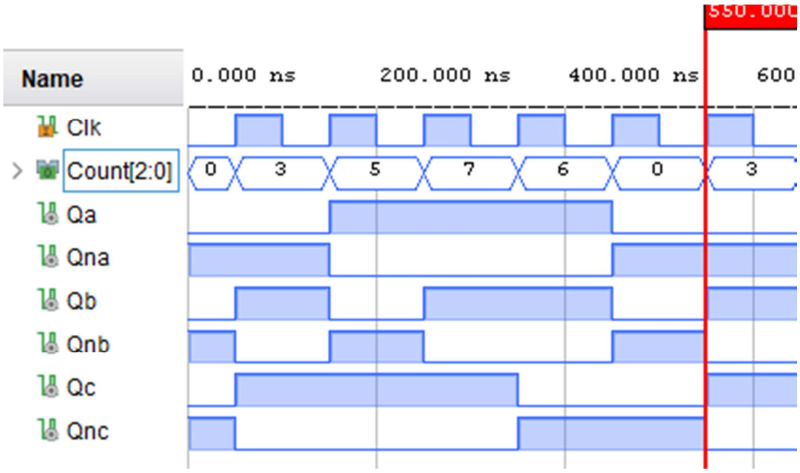


Figure 3.17: Functional behavior of synchronous counter

4.0 TUTOR MARKED ASSIGNMENT

It is desired that a synchronous counter performs the sequence of count 0000 to 0001… to 1001 and then return to 0000. The characteristic equations for the operation of the counter are:

J1 = K1 = 1
J2 = Q1Q4□'
K2 = Q1
J3 = K3 = Q1Q2
J4 = Q1Q2Q3
K4 = Q1

Draw a circuit for the counter based on the characteristic equations.

5.0 CONCLUSION

In this unit, you have been introduced to sequential circuits and their governing truth tables. You have also been shown how simple sequential components can be interconnected to design more advanced and useful sequential circuits.

6.0 SUMMARY

The unit has been able to show to the reader how the theoretical knowledge of basic sequential circuits can be used in designing circuits with a desired functionality. The reader has also been shown the central role truth tables play in understanding and using sequential circuits.

7.0 REFERENCES/FURTHER READING

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Malvino, A. P. (1999). Digital Computer Electronics. 3rd Ed. McGraw Hill. ISBN: 0-02-800594-5

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UNIT 2 SEQUENTIAL CIRCUITS – ASYNCHRONOUS: ANALYSIS PROCEDURE, RACE CONDITIONS, STABILITY CONSIDERATIONS

CONTENTS

1.0 INTRODUCTION

Asynchronous sequential circuits (ASC) are a special class of sequential circuits that do not use clock pulses. The change in their internal states occurs as a result of a change in input variables. In contrast to synchronous sequential circuit (SSC) that use clocked flip-flops as memory elements, ASCs use un-clocked flip-flops called latches or time delay elements. It should be noted that the memory capability of time-delay elements is a function of the time taken for a signal to propagate through its digital gates. Conceptually, the ASC as depicted in figure 3.1 resembles a combination with a feedback.

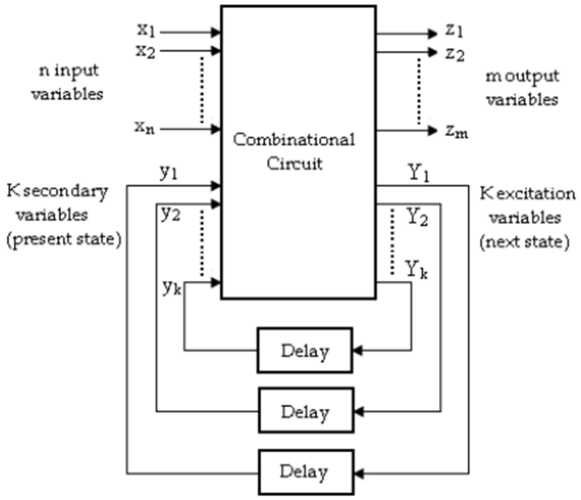


Figure 3.1: Conceptual representation of an ASC

The ASC shown in figure 3.1 has two sets of inputs, the first being external to the circuit, and the second being the feedback input that

represent the present state of the circuit. Similarly, two sets of outputs characterize the output of the circuit; the first being the output from the circuit, and the second is the output that serve as an input to the feedback loop.

2.0 INTENDED LEARNING OUTCOMES (ILOS)

The student is expected at the end of this unit to be able to have a good understanding of ASC, its area of application, design methodology, and important considerations that must be made when designing ASC circuits.

3.0 MAIN CONTENT

3.1 Analysis Procedure

ASC are usually analyzed by deriving a transition table that characterizes the sequence of internal states and outputs as a function of the changes that occur in the input variables. Consider the circuit shown in figure 3.2.

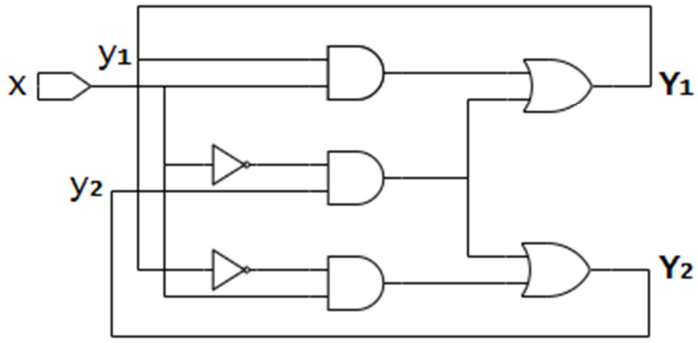
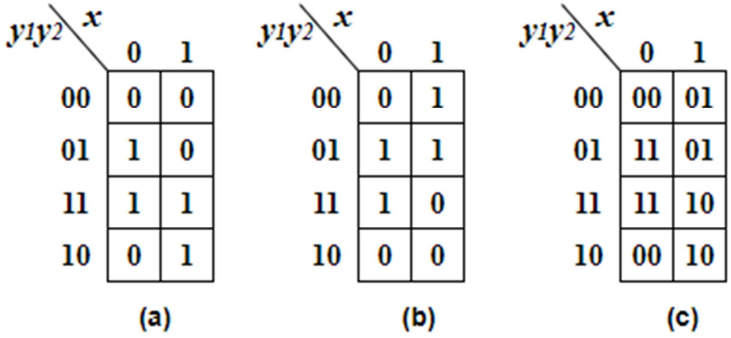


Figure 3.2: An ASC circuit

The circuit in figure 3.2 has two feedback loops via the OR gate outputs which terminate at the AND gate inputs. The circuit also has one input variable x and two internal states that are excited by two variables Y1 and Y2 (next state), and two secondary variables y1 and y2 (present state). The propagation delay from a y input to a corresponding Y output form the delay of the feedback loop. The standard delay values for the logic gates ranges between 2 to 10ns, and the connecting wires 1ns.
For the circuit in figure 3.2 under consideration, the Boolean equations are as follows:

$$Y_1 = xy_1 + x'y_2$$
$$Y_2 = xy_1' + x'y_2 \qquad (3.1)$$

From equation 3.1, the maps for Y1 and Y2 are derived as shown in figure 3.3a-b, while figure 3.3c shows the transition table that is derived by the combination of the values in figures 3.3a-b.



y_1y_2 \ x	0	1
00	0	0
01	1	0
11	1	1
10	0	1

(a)

y_1y_2 \ x	0	1
00	0	1
01	1	1
11	1	0
10	0	0

(b)

y_1y_2 \ x	0	1
00	00	01
01	11	01
11	11	10
10	00	10

(c)

Figure 3.3: Characteristics map and transition table (a) Map for $Y_1 = xy_1 + x'y_2$ (b) Map for $Y_2 = xy' + x'y_2$ (c) Transition table

From figure 3.3c, a state table for the circuit is derived as shown in Table 3.1 where the stable states i.e. y1y2x = 000, 011, 110, and 101 are indicated in yellow. Similarly, the unstable states i.e. y1y2x = 001, 010, 111, and 100 are indicated in blue. Figure 3.3 shows the waveform verification of Table 3.1.

Table 3.1: State table for ASC circuit

Present state		Next state			
		x = 0		x = 1	
0	0	0	0	0	1
0	1	1	1	0	1
1	0	0	0	1	0
1	1	1	1	1	0

Stable state
Unstable state

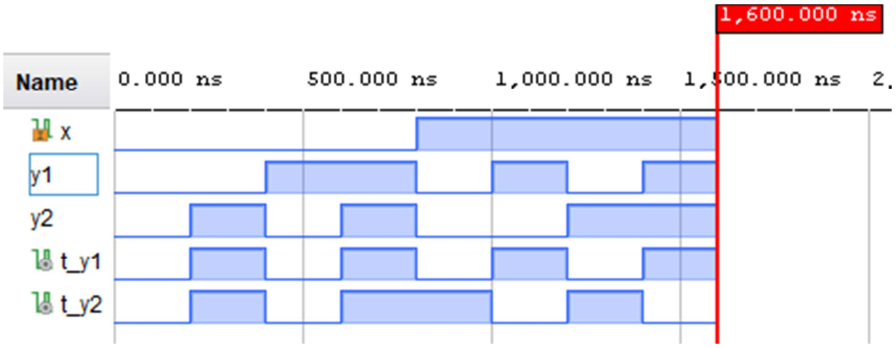


Figure 3.1: Waveform verification of ASC circuit

Formally, the following steps govern the derivation of the state table:
Evaluate all the feedback loops in the circuit
All output variables should be designated Yi, and the corresponding input variables yi for i = 1,2,…,k, with k representing the total number of the circuit feedback loops.
Derive all the Boolean functions of Y's, with respect to external inputs and y's.
For each Y, plot a function map such that the y variables define the rows, and the external inputs define the columns
Derive the transition table through the combination of all map into a single table where each square is defined as Y = Y1Y2…Yk
Identify the stable the states by matching the values of the next state that have the same value as the present state in a given row, and unstable states when the opposite is the case.

3.2 Race Conditions

In ASCs, a race condition is a situation when a change in the input variables causes two or more binary state variables to change value. The change in state variables is usually unpredictable when unequal delays characterize the race condition. As an example, if it is desired that a state variable changes from the value 00 → 11, unequal delays will trigger a transition 00 → 10 → 11 when the latency of the first variable is less than the second variable, and 00 → 01 → 11 when the latency of the second variable is less than the first variable. Consequently, a priori knowledge of the order by which state variables will change is likely to be impossible. However, if the final state of the circuit is not affected by the order in which the state variables change, then the condition is called noncritical race. If the reverse is the case, then a critical race has occurred, and this should be avoided at all costs.

3.3 Stability Considerations

Stability conditions are an integral part of the design procedure for ASCs in order to ensure stability and prevent oscillation of the circuit between unstable states due to unstable condition. A key methodology used for the detection of instability is the use of transition table analysis. Consider the circuit shown in figure 3.4 alongside its excitation function. The transition table is shown in figure 3.5.

$$Y = (x_1 y)' x_2 = (x_1' + y') x_2 = x_1' x_2 + y' x_2$$

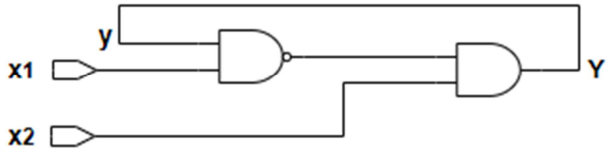


Figure 3.4: ASC circuit

y \ x1x2	00	01	11	10
0	0	1	1	0
1	0	1	0	0

Figure 3.5: Transition table

In the transition table of figure 3.5, the stable states i.e. when Y = y are circled, while the un-circled states represent unstable states. It can be observed for column x1x2 = 11, unstable state exists; consequently, the values of y and Y are always opposite. For example, when y = 0, then Y = 1; a table occurs in the second row of the column. When the reverse is the case, the transition reverts back to the first row. Hence, as long as x1x2 = 11, an oscillation occurs infinitely between 0 and 1.

4.0 TUTOR MARKED ASSIGNMENT

An ASC circuit is defined by the following excitation equations:

$$Y_1 = xy_1 + xy_2$$
$$Y_2 = xy_1' + xy_2$$

Draw the ASC circuit represented by the equations
Derive the map for the two equations and draw the transition table from the map.

5.0 CONCLUSION

In this unit, you have been introduced to ASC circuits and the standard methodology for the analysis of ASC circuits. You have also been presented with two critical design factors for ASC circuits i.e. race conditions, and stability considerations.

6.0 SUMMARY

The unit has been able to show to the reader the theoretical knowledge of ASC circuits. The reader has also been shown the central role transition tables play in understanding of ASC circuits.

7.0 REFERENCES/FURTHER READING

Ferdjallah, M. (2011). Introduction to Digital Systems: Modelling, Synthesis, and Simulation using VHDL. Wiley, ISBN: 978-0470900550